Professional Radio Applications

PLESSEY
Semiconductors

This application note describes the use of integrated circuits manufactured by Plessey Semiconductors in Professional Radio applications.

Development of new circuits for this field of application continues. The Customer Services Manager, Plessey Semiconductors Ltd. should be contacted to obtain details of new products.

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Section 1

Radio Linear Circuits

Radio Linear Circuits

INTRODUCTION TO SL600 AND SL1600 SERIES

Plessey Semiconductors originally developed the SL600 series for use in military SSB systems. For such applications, hermetic packages and full-temperature operation are necessary: the SL600 series devices meet such specifications. As the range expanded, requirements arose for less expensive versions of SL600 devices and the SL1600 series was introduced. The SL1600 series consists of the same chips as are used in the SL600 series but packaged in plastic DIL packages (mostly 8-lead minidips) tested to less stringent specifications, and supplied with a —30°C to +70°C temperature specification. In a few cases some of the pins present in the SL600 devices are omitted in the SL1600 devices in order to allow a chip previously supplied in a 10-lead TO-5 to be encapsulated in an 3-lead minidip.

SL600 and SL1600 type numbers are used in section headings but to avoid tedious repetition, only the SL600 type numbers will be used in the text unless there are significant differences between the SL600 and SL1600 devices. Pin numbers generally refer to both types; in cases where pin numbers differ, the pin numbers for the SL1600 device is given in brackets, e.g. Pin 6(7).

SL600/1600 PRODUCT RANGE

AMPLIFIERS	SL610 SL611 SL612	SL1610 SL1611 SL1612	140MHz, 20dB 100MHz, 26dB 15MHz, 34dB
MIXERS	SL640 SL 641	SL1640 SL1641	
DETECTORS AND AGC GENERATORS	SL621 SL623	SL1621 SL1623 SL1625	AGC from detected audio AMSSB detector and AGC from carrier AM detector and AGC from carrier
AUDIO	SL630	SL1630	200mW headphone amplifier

SL610C, SL611C, SL612C, SL1610C, SL1611C & SL1612C

RF/IF amplifiers

The SL610C, SL611C and SL612C integrated RF amplifiers are similar circuits, having typical voltage gains of 10, 20 and 50 and upper 3dB gain points at 140MHz, 100MHz and 15MHz respectively. The first two draw a supply current of about 15mA at 6V and have some 50dB AGC range while the SL612C draws 3.5mA and has 70dB of AGC. All three are intended to use with +6V supplies and have internal decoupling. They will drive an output signal of about 1V rms.

The cross-modulation of the circuits is 40dB down on signal at 1V rms output with no AGC, and at 250mV rms input with full AGC. The input and output admittances of the circuits are not greatly affected by AGC level.

CIRCUIT APPLICATIONS

There are seven connections to each circuit: an input, an input bias point, an AGC input, the output, the positive supply pin and two earths — for input and output respectively.

The positive supply should be 6V, but the devices will function at supplies of up to 9V. Since internal HF supply decoupling is incorporated a certain amount of HF ripple can be tolerated in the supply. LF ripple should be kept down as it can cause intermodulation — especially at large HF signal levels — and 10mV rms of LF ripple should be considered a maximum.

The AGC characteristic is shown in Fig. 1. It is temperature dependent, so that while a potentiometer may be used to provide a gain control voltage the gain so defined will not be temperature stable to better than ± 2dB. The AGC terminal will normally draw about 200 microamps at 5V — in some SL610C and SL611C devices this may be as high as 600 microamps.

There are two earth connections: pin 4 is the input earth and pin 8 the output earth. When several devices are cascaded pin 8 of one stage and pin 4 of the next should have a common earth point — also high common earth impedances to pin 4 and pin 8 of the same device should be avoided. Fig. 2a shows a circuit where common earth impedance could cause instability and Fig. 2b shows one where the input and output signals have correct point earthing. If extra supply decoupling is used the capacitor should ground to the output earth point. The can should be separately earthed in applications at VHF or in the presence of a large RF field.

The input bias point (pin 6) is normally connected directly to the input (pin 5) and the signal applied through a capacitor but occasionally, when the signal is obtained from a tap on a coil, the arrangement in Fig. 2b may be used to give slightly improved noise performance. C_D is a decoupling capacitor. The SL610/611 noise figure is approximately 4dB at 300 ohms source impedance and 6dB at 50 ohms and at 2.5 kilohms the noise figure for the SL612 is 3dB at 800 ohms source impedance.

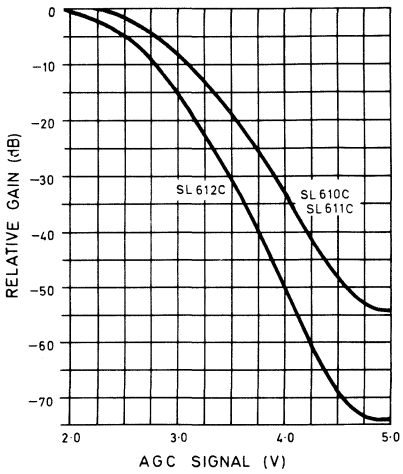


Fig. 1 SL610/11/12 AGC characteristics

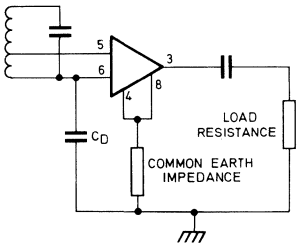


Fig. 2(a) Incorrect connections of earths

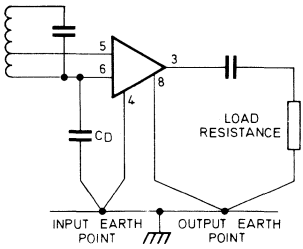
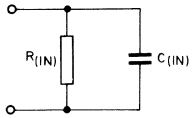
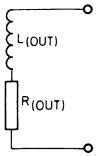


Fig. 2(b) Correct connection of earths



(a) input circuit



(b) Output circuit

Fig. 3 Equivalent circuits

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Figs. 3a and 3b and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Figs. 4 and 5. It will be seen that for the SL610C and the SL611C, R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700kHz.

If an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and if R1 is higher than R_{in}. Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input is inductive, therefore, it may be shunted by a 1k resistor; where the load is capacitive, 47 ohms should be placed in series with the output.

Suitable input arrangements for the amplifiers are shown in Fig. 2b and Fig. 6. The method shown in Fig. 6a is representative of all inputs — the input and bias points are directly-connected and the signal is coupled via a capacitor. If the input is inductive the 1k resistor shown in Fig. 6b may be required, although usually it can be omitted. If a crystal filter is used it should be correctly terminated, allowing for the impedance of the IC, and coupling made via a capacitor.

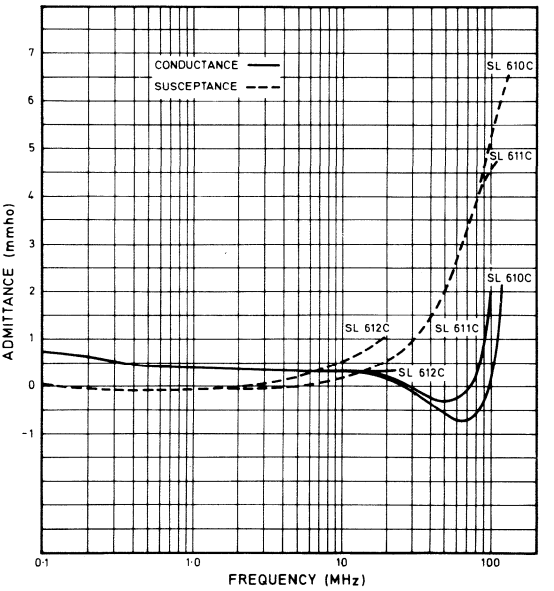


Fig. 4 Input admittance with o/c output (G_{11})

The output is a voltage source, with the impedance characteristics mentioned above. Output coupling is via a capacitor, with a series resistor if necessary to preserve stability (Fig. 6c). If a current output to a tuned circuit is required the arrangement in Fig. 6d is suitable, using almost any small signal NPN transistor with an f_T of over 300MHz and low C_{OB}. To drive particularly low impedances, e.g. a 50 ohm coaxial cable, this impedance should be increased somewhat by a series output resistor (say, 100 ohms) as, if the output is loaded directly by low impedance, most of the negative feedback will be removed — with consequently poor linearity and constancy of gain. Examples of the use of these amplifiers are shown in Fig. 7.

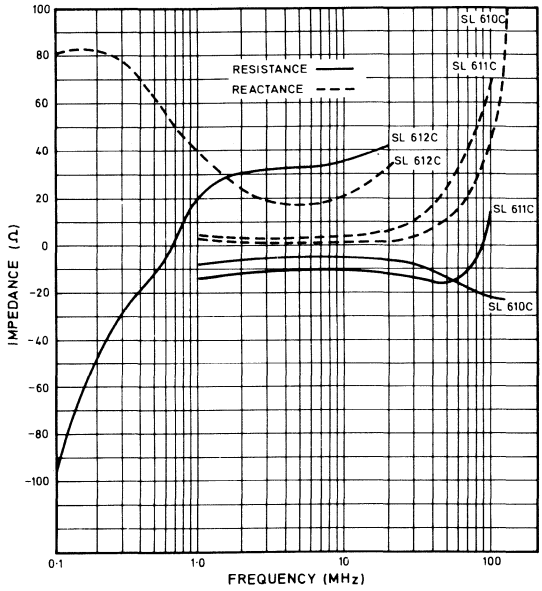
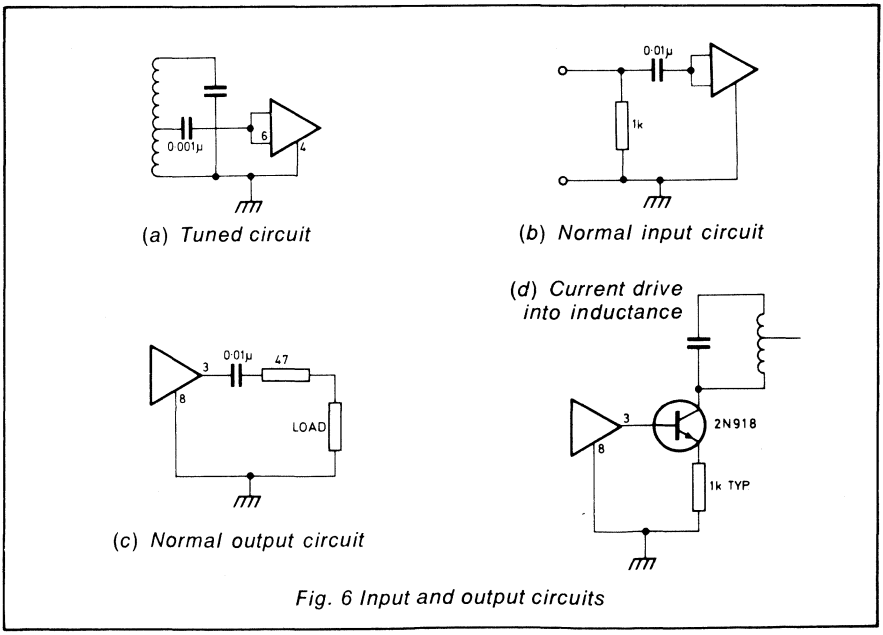


Fig. 5 Output impedance with s/c input (G_{22})



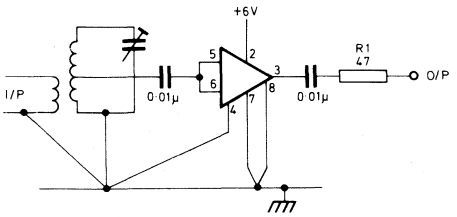
(a) *Tuned circuit*

(b) *Normal input circuit*

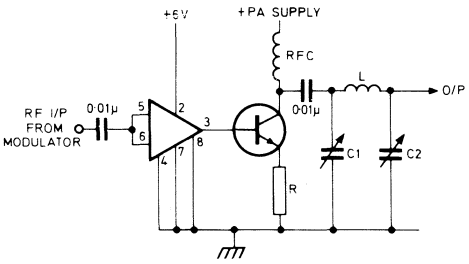
(c) *Normal output circuit*

(d) *Current drive into inductance*

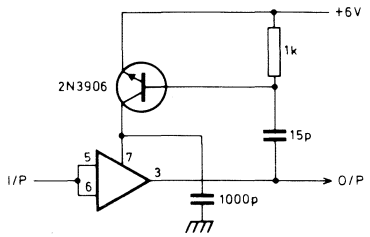
Fig. 6 Input and output circuits



(a) *RF preamplifier. Use SL610C up to 140MHz, SL611C up to 70MHz, SL612C up to 12MHz. R1 may be omitted if the load is neither capacitive nor very low impedance.*



(b) *Linear power amplifier for low power SSB transceivers. L, C1 and C2 form the output π tank circuit. The values of PA supply and R should be chosen to suit the transistor used. C_{ob} should be as low as possible.*



(c) *Constant level RF amplifier stabilising at approximately 500mV rms output over a range of inputs greater than 20dB. SL610C, 611C or 612C may be used. With tuned feedback, this circuit makes an excellent constant level oscillator.*

Fig. 7 SL610/11/12

Double balanced modulators

PRINCIPLES OF OPERATION

A simple double-balanced modulator is shown in Fig. 8 . It is evident that the sum of the two output currents equals the tail current and that, from considerations of symmetry, if either V1=V2 or V3=V4 then I1=I2. Also if R is much greater than R_e the collector currents of TR1 and TR2 will differ by an amount proportional to the difference between V1 and V2. If, therefore, a small input at frequency f_1 is applied between V1 and V2 and a large signal at f_2 is applied between V3 and V4, sufficient to turn the transistors TR3, TR3, and TR4, and TR4, fully on and off, it is evident that switching modulation, similar to that of a diode ring will occur and frequencies $|f_1 \pm f_2|$ will occur at the output as will sums and differences of f_1 and the odd harmonics of f_2 i.e. $|f_1 \pm 3f_2|$, $|f_1 \pm 5f_2|$, etc.

CIRCUIT DESCRIPTION AND APPLICATIONS

The circuits of the SL640C and SL641C are very similar but have different signal input and output configurations — these are fully discussed below.

The circuits require a single, well-decoupled positive supply of between 6 and 9 volts and consume about 12mA. Pin 2, an internal bias point, must also be decoupled by a low-leakage (less than 100nA) capacitor having a low reactance at the lowest signal or carrier input frequency.

Pin 1, which is connected to the can, should be earthed to prevent HF pickup.

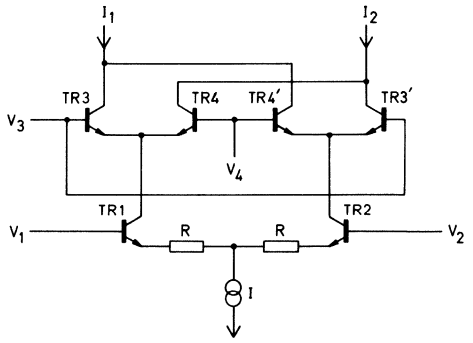


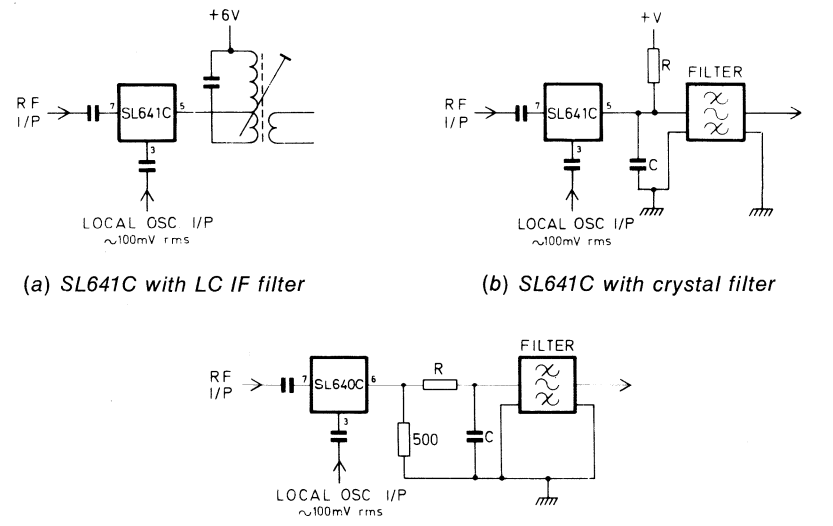
Fig. 8 A transistor double-balanced modulator

The input and carrier signals, which should not exceed 200mV rms, are applied to pins 7 and 3 respectively. Both the SL640C and the SL641C have a carrier input impedance of 1 kilohm and 4pF and the SL641C has a similar signal input impedance. The signal input impedance of the SL640C is 500 ohms and 5pF. The input coupling capacitors should have a leakage of less than 100nA and an impedance of less than 100 ohms at the lowest frequency they will carry. This should be reduced to less than 10 ohms above 10MHz.

The output of the SL641C is intended as a current drive to a tuned circuit. If both sidebands are developed across this load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course, increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output, which requires a discrete load resistor of not less than 560 ohms. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

The circuits will operate with input frequencies between 1Hz and 70MHz with the specified performance; the SL641C will operate at up to about



(a) *SL641C with LC IF filter*

(b) *SL641C with crystal filter*

(c) *SL640C with crystal filter*

Fig. 9 SL640/41C receiver mixer circuits

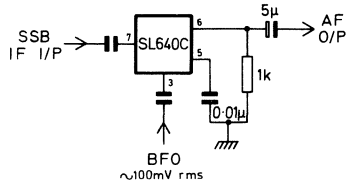
150MHz with reduced performance. To use them at frequencies below 100Hz precautions must be taken to prevent leakage in the input coupling capacitor from altering the device bias.

Some applications of the SL640C and SL641C are shown in Figs. 9 and 10 Power, decoupling, and earth connections are not shown.

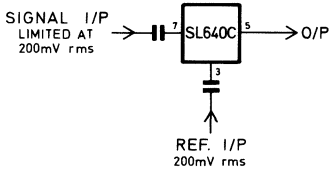
Fig. 9a shows the SL641C used as a receiver mixer driving a wound IF coil. Fig. 9b shows it driving a crystal filter. R and C must be selected to match the filter. If R is less than 800 ohms it may be connected to the +6V line supplying power to the SL641C; if it is between 800 ohms and 1.8 kilohms it should be connected to +9V (while the SL641C supply must remain at +6V). If R is greater than 1.8 kilohms the circuit in Fig. 9b is unsuitable and the SL640C circuit illustrated in Fig. 9c should be used.

The SL640C and SL641C have a noise figure of about 10dB at 100 ohms source impedance. When used as receiver mixers they have better than —40dB intermodulation products so long as unwanted signals do not exceed 30mV rms. Thus, either can be used as a receiver mixer at HF without an RF amplifier since atmospheric noise will far exceed device noise at these frequencies if the antenna is reasonably good. If an SL610C RF amplifier is used the intermodulation threshold will be reduced to 3mV rms (since the SL610C has a gain of 10). The SL640/41 is then less attractive as a mixer and a diode ring mixer should be used.

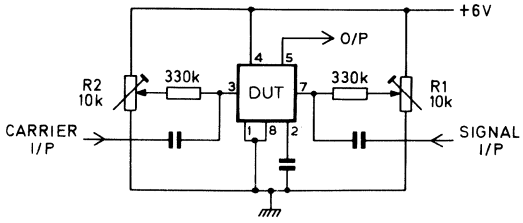
Fig. 10a shows the SL640C used as an SSB detector. The capacitor connected to output pin 5 decouples the sum frequency $|f_1 + f_2|$, while the audio difference frequency $|f_1 - f_2|$ is taken from pin 6. The phase comparator shown in Fig. 10b is more useful — it may be used as a detector for phase modulated signals or as a comparator in phase-locking systems such as frequency synthesisers.



(a) *SL640C SSB detector*



(b) *SL640C phase comparator*



(c) *Signal and carrier leak adjustment*

Fig. 10 SL640/41C detector circuits

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig. 10c. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

Fig. 11a shows the SL640C or SL641C used as a sideband generator. Both sidebands are produced so that if a single sideband is required it must be obtained by subsequent filtering (Fig. 11b). If pin 2 is earthed by a resistor of about 15 kilohms (its actual value may need to be selected) the device's carrier leak is increased to a point where the DSB signal becomes AM. This is useful where it is desired to select sideband or AM. In the circuit shown in Fig. 11c a single sideband only is produced. It is important that both the audio and carrier reference and quadrature signals should be accurately 90 degrees out of phase. The amplitude of one phase of audio should be adjusted to obtain maximum second sideband rejection.

If the carrier reference is connected to input A, and the carrier quadrature to input B, LSB output results. If the carrier quadrature is connected to input A, and reference to input B, USB output results.

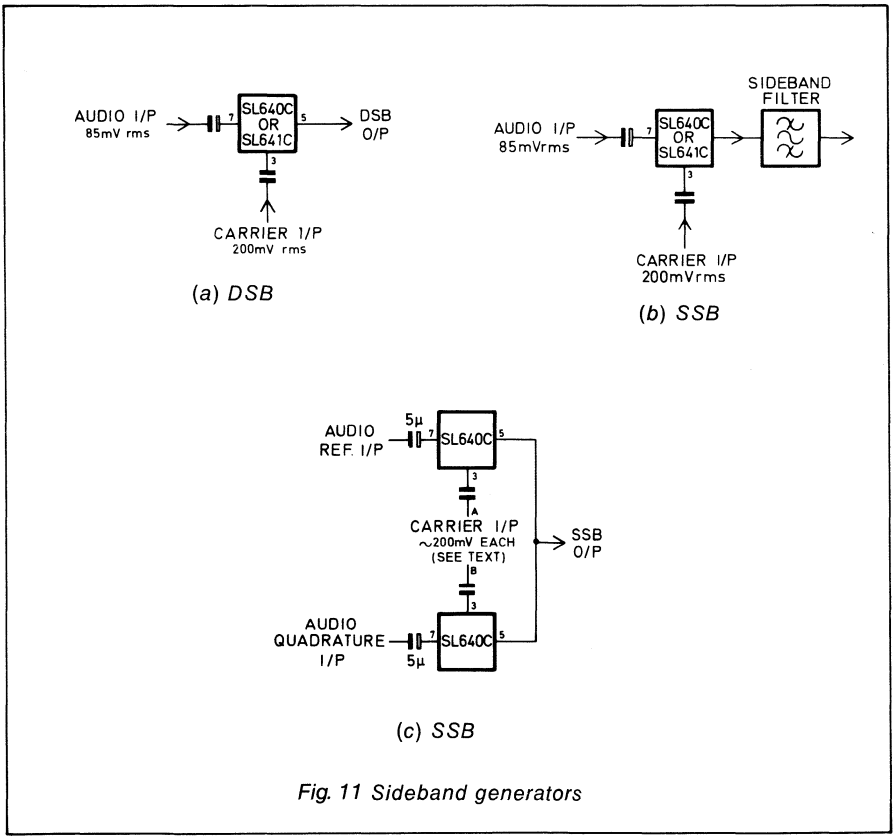


Fig. 11 Sideband generators

SL621C & SL1621C

AGC generators

The SL621C is an audio-operated AGC generator designed for use with the SL610/11/12 RF amplifiers in SSB receivers.

An ideal single sideband AGC generator must set the AGC rapidly when a new signal appears and follow a rising or fading signal but, if the signal disappears altogether (as in pauses in speech), retain the AGC level until the signal recommences. If the signal remains absent for more than a preset time, however, the system should rapidly revert to full gain. The SL621C will perform these functions and will also produce short-lived pulses of AGC to suppress noise bursts.

CIRCUIT DESCRIPTION

The operation of the circuit is described with reference to Fig. 12, which also illustrates the dynamic response of a system controlled by an SL621C AGC generator.

The SL621C consists of an input AF amplifier, TR1-TR4, coupled to a DC output amplifier, TR16-TR19, by means of a voltage back-off circuit, TR5, and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

An audio signal applied to the input rapidly establishes an AGC level, via TR14, in time t_1. Meanwhile the long time constant detector output (TR15) will rise and after t_3 will control the output because this detector is the more sensitive. If the signals at the SL621C input are greater than approximately 4mV rms they will actuated the trigger circuits TR6-TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate which corresponds to a rise in receiver gain of 20dB/sec. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as in pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector (TR14) falls to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, thus holding off TR12 via TR11. When the pulses cease, C3 discharges and after t_5 turns on TR12, rapidly discharging C2 (in time t_4) thus restoring full receiver gain. The hold time, t_5, is approximately one second with C3=100 microfarads. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses. Fig. 12 also shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

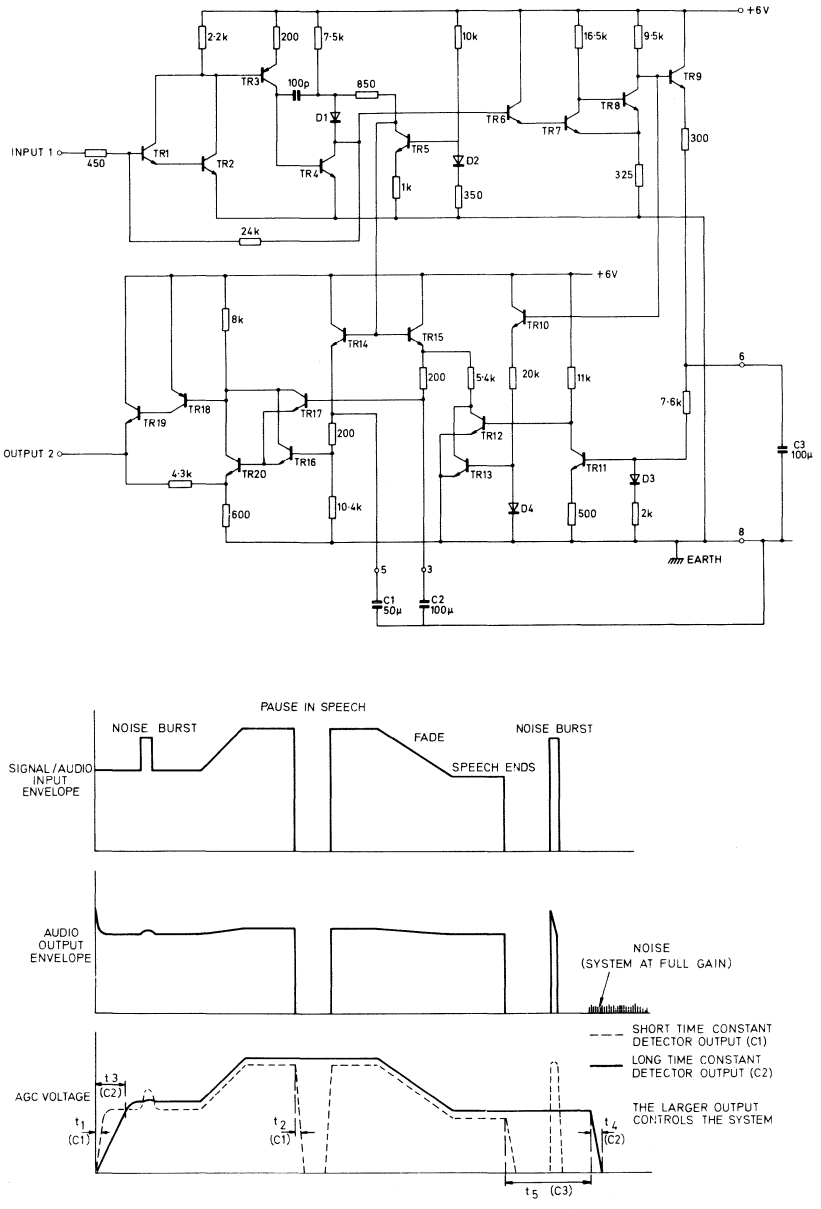


Fig. 12 Circuit diagram of SL621C and dynamic response of an AGC system controlled by an SL621C

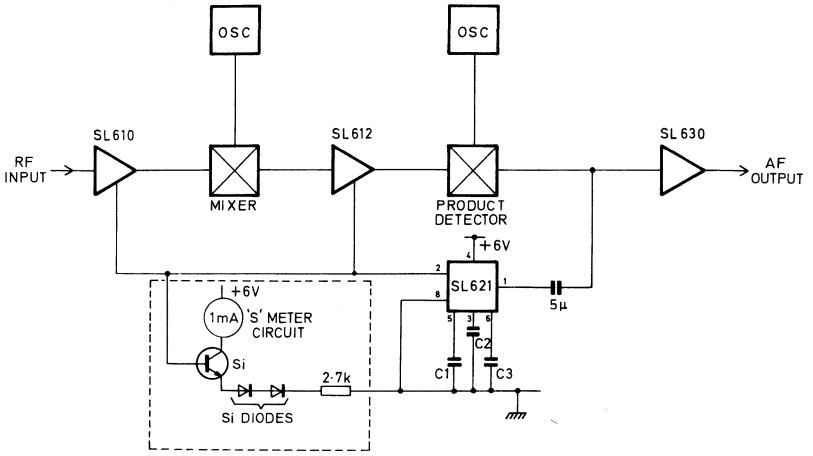


Fig. 13 An SL621C used to control an SSb receiver

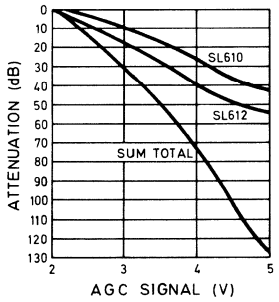


Fig. 14 Attenuator AGC signal

The various time constants quoted are for C1=50 microfarads and C2=C3=100 microfarads. These time constants may be altered by varying the appropriate capacitors.

CIRCUIT APPLICATIONS

The SL621 is used in an SSB receiver as shown in Fig. 13. AGC need only be applied to two of the gain stages even if there are more than two such stages in the receiver since AGC applied to two stages only will result in over 120dB AGC range. It is usual to apply AGC to the first RF stage and the first IF stage and it will be seen from Fig. 14 that an SL612 IF amplifier reacts earlier to an increasing AGC voltage than an SL610C RF amplifier. This has the effect of delaying the AGC to the input stage, thus improving the receiver signal to noise ratio at low AGC levels.

Fig. 14 also shows the total attenuation to be expected at any AGC voltage when AGC is applied to one SL610C and one SL612C in a system; from this one can calculate the calibration of an 'S' meter for use with the SL621C. Such a meter, as shown in Fig. 13, should have a sensitivity of 2.6V FSD and be calibrated linearly from 0 to 120dB.

The output current capability of the SL621 is not high and it should not be expected to drive more than three SL610/11/12 devices in addition to an 'S' meter circuit similar to that shown in Fig. 13.

There are two other important points to observe when using the SL621C: supply de-coupling and input coupling. Since capacitors C1 and C3 may need to charge very quickly, the source impedance of the 6V supply line at low frequencies should be very low, if necessary being decoupled by a low impedance 1000 microfarad capacitor placed near the SL621C.

The input should be applied to pin 1 via a capacitor of not more than 470 ohms reactance at the lowest input frequency encountered, and should never exceed 1Vrms. Input voltages in excess of this level may cause the internal amplifier to block, with consequent failure of the AGC voltage. The condition can be avoided, if necessary, by using a diode limiter at the input.

In the presence of RF fields the AGC line may need to be decoupled: a 5000pF capacitor from pin 7 of each RF amplifier to earth and a 100 ohm resistor from each pin 7 to the AGC line should be adequate. It is, however, important not to use a capacitance greater than 15000pF, otherwise the impulse suppression characteristic of the circuit will be degraded.

The SL621 may be used with supply voltages between +6V and +9V.

SL623C, SL1623C & SL1625C

AM detector, AGC amplifier and SSB demodulators

The SL623C consists of an AM detector, an SSB detector and an AGC generator designed for use with AM. The SL623C was introduced to enable the small-signal sections of an HF AM/SSB transceiver to be completely integrated — all functions with the exception of the power amplifier can be realised with SL600 series integrated circuits. The outputs of the SL623C will drive most audio output stages with input impedances over 10 kilohms, and are particularly suitable for driving the SL630C.

In addition to its audio outputs, the SL623C AGC generator is designed to control SL610/11/12 RF/IF amplifier strips, but, unlike the SL621C AGC generator, which operates from an audio signal, the SL623C control voltage is carrier-derived. It is therefore less suitable for use with SSB or CW. However, the AGC output pins of an SL621C and an SL623C may be connected together for an SSB/AM receiver, the gain then being controlled by the device with the higher output voltage.

The SL1625C is an SL1623C without its SSB detector.

CIRCUIT DESCRIPTION (Fig. 15)

The IF input is applied directly to one input of a full-wave detector and, via a unity-gain inverting amplifier, to the other input of the full-wave detector and to the signal input of a balanced demodulator. Two outputs from the full-wave detector are brought out of the package: audio and AGC. The AGC signal is used as the input to the AGC amplifier of the device. The AGC amplifier consists of two amplifiers in series. The first has a gain which may be varied between —0.25 and —5 by an external resistor and the second has a fixed gain of —20 and a frequency compensation point. The SSB detector, which requires a carrier input of 100mV rms, consists of a simple balanced demodulator.

A single positive supply of between +6V and +9V is required. The supply should be decoupled close to the can by a 0.1 microfarad capacitor. Current consumption is approximately 10mA at 6V supply and zero AGC voltage, but rises with both supply voltage and AGC output level.

CIRCUIT APPLICATIONS

AM Detector

The detected AM output has an output impedance of about 1 kilohm and should be decoupled at RF with a 0.01 microfarad capacitor (C1). It should be connected to the audio stage via a dc blocking capacitor. The other detector output is similar but should be decoupled with a 50 microfarad capacitor (C2) to remove AF, and connected via a preset potentiometer R28 to the AGC amplifier input to provide rectified carrier for amplification as AGC. C1 and C2 should be connected directly to the earth pin via the shortest possible leads, which should not be common to any other components. C2 should have an AF series resistance of under 1 ohm and, if it does not also have a low RF impedance, should be shunted by a 0.01 microfarad RF bypass capacitor (C3). These measures prevent instability due to possible RF current loops.

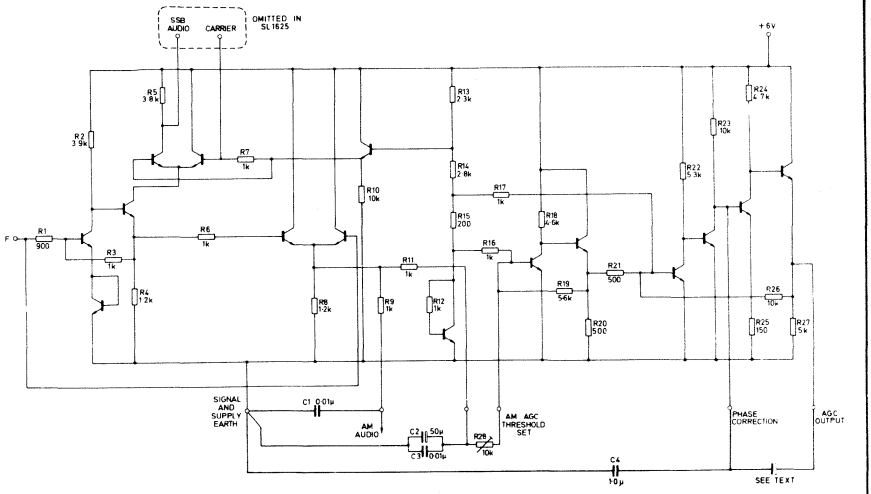


Fig. 15 SL623C circuit diagram

AGC Generator

Pin 3, the AGC amplifier phase correction point, should be decoupled to ground by a 1 microfarad capacitor (C4) ,keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

A capacitor connected to the phase correction point and the output of the AGC amplifier helps to reduce the ripple on the AGC output. Its value varies from system to system and with intermediate varying frequencies. Normally-used values vary between 0.1 and 10 microfarads. As there is no easy way to predict suitable values for particular systems, this component must be 'selected on test'.

The AGC output (pin 4) will drive at least two SL610/11/12 amplifiers and the 'S' meter circuit shown in Fig. 13. The SL623 AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623C will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer R28 is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

SL630C & SL1630C

Microphone/headphone amplifier

The SL630C is an audio amplifier having 40dB gain and an internal gain control of approximately 60dB, and an output capability of 200mW into a 40 ohm load when used with a 12V supply.

CIRCUIT DESCRIPTION AND APPLICATIONS

To maintain HF stability — particularly on negative half-cycles — the output (pin 1) should be decoupled by a 1,000pF, low series inductance, capacitor placed directly between pins 1 and 10 (8) with leads cut as short as possible. This component must be on the integrated circuit side of the output coupling capacitor. At high supply voltages and/or low temperatures 10 ohms must be placed in series with this capacitor and 100pF connected from pin 4 to earth. The output is coupled to its load with a capacitor of a low impedance relative to the load at the lowest frequency to be used. The load may be resistive or reactive and, for maximum power output, should lie on the load/supply voltage line. *Any higher value of load impedance is quite safe but the device will over-dissipate and eventually destroy itself by overheating if the output is short-circuited.* The optimum load therefore, at any rate with supplies of over 9V, can be regarded as a safe minimum. The circuit shown in Fig. 16 which shows the SL630C used as a headphone amplifier, may also be used with loudspeakers having suitable impedances. The distortion is about 0.5 per cent at full output.

The power supply, to pin 2, should be between +6V and +12V and adequately decoupled both at HF and LF. The quiescent power consumption at various supply voltages is shown in the Power characteristics, as is the relation of the supply voltage to the optimum load and the maximum power available.

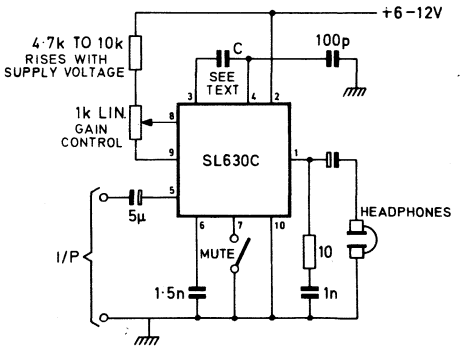


Fig. 16 Headphone amplifier using the SL630C

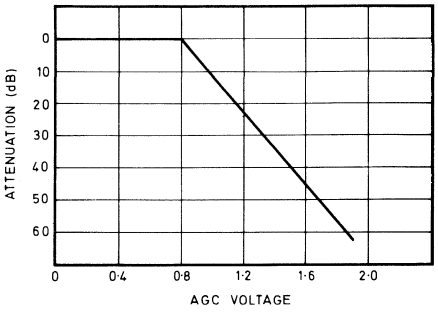


Fig. 17 AGC characteristics

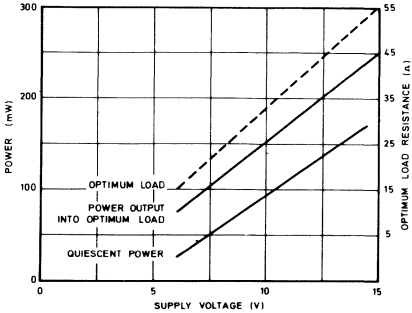


Fig. 18 Power characteristics

A capacitor connected to pins 3 and 4 defines the high frequency response of the amplifier. The upper 3dB frequency, f, is given by the formula:

$$f = \frac{16000}{C+20} \text{ kHz. (C is in picofarads)}$$

Pins 5 and 6 are input terminals. They may be used together as a differential input, in which mode they present an impedance of approximately 2 kilohms and result in a voltage gain (without gain control) of 100 (40dB). When the input is obtained from a magnetic transducer or a transformer it is desirable to use the differential input mode since the signal winding may be connected directly between pins 5 and 6 and no other components are required.

An input may also be applied between pin 5 and earth. In this case the gain is 200 (46dB) and the input impedance 1 kilohm. Pin 6 should be earthed by 1500pF. A coupling capacitor is required between the input and pin 5.

The circuit is muted by earthing pin 7. A muted circuit attenuates an input by about 100dB. There is no mute facility on the SL1630.

Gain control is applied to pin 8, (7) which has an input impedance of 3.6 kilohms. It must be appreciated that even with full gain control the input cannot exceed 50mV rms without clipping so that at high control levels the output level is limited. The AGC characteristics will vary with temperature but, as shown in Fig. 16 a potentiometer to give manual gain control can be connected to the internal bias point at pin 9 which provides a temperature-compensated reference at the voltage at which gain control commences. This reference pin is omitted on the SL1630C. Pin 10 (8) is the signal earth and negative power supply connection.

Application—SL600 Series

SSB TRANSCEIVER USING SL600 SERIES

This transceiver, shown in Fig.19, consists of a single conversion superhet receiver with a 9MHz IF and a very efficient audio-derived AGC system, and a filter type SSB generator, also working at 9MHz. Audio AGC in the modulator path gives constant level output. The transmitter and receiver are arranged so that no signal switching is required between transmit and receive, and the RF components are common to both.

The RF input is direct to an Anzac MD-108 (or similar) hot carrier diode ring mixer. This has 50 ohm ports and is also driven by the local oscillator, at about +7dBm (500mV). The output is connected via a 3: 1 step-up transformer to a 9MHz crystal filter. This filter has the 2.4kHz bandwidth required for SSB and a 90dB stopband. Filters with 60dB stopband can be used, but additional filters may be required at low local oscillator frequencies to keep the local oscillator signal out of the IF amplifier (and the overall receiver performance will, of course, be degraded).

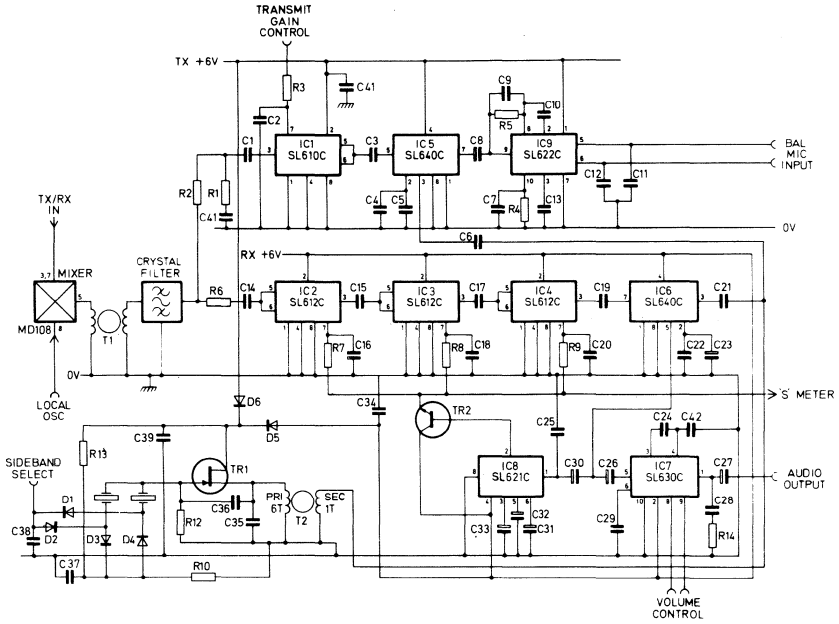


Fig. 19 Simple SSB transceiver circuit

Note: SL6270 can be used in place of SL622

The filter used, an SEI QC1246AX or a KVG XF9-B, has a terminating impedance of 500 ohms, but only within the passband of the filter. At frequencies outside the passband it may be very different, which means that the impedance that the filter presents to the diode ring mixer via the transformer will vary from 50 ohms. Such a mismatch will degrade the cross-modulation and carrier leak performance of the diode ring. However, it was decided on balance, that it was better to tolerate such degradation — which is not excessive — than to complicate the design by incorporating a broadband impedance match (which would probably not be bidirectional and hence would have to be switched between transmit and receive).

The present design allows the same arrangement to operate in opposite directions during receive and transmit without any switching. On the other side of the crystal filter the transmit and receive signal paths diverge but are still not switched.

The Receiver

The incoming RF signal is mixed with the local oscillator in the mixer described above and then passes through an SSB bandwidth 9MHz crystal filter. It is then amplified by three cascaded SL612CIF amplifiers, IC2, 3 and 4. These amplifiers are untuned and since the strip has a maximum gain of 102dB careful attention must be paid both to noise and to stability. The SL612C has a 3dB noise figure which means that the broadband noise at the output of the three-stage strip is about 10mV RMS. This is not sufficient to affect a product detector, which is only concerned with the component within a few kHz of the BFO frequency, but would cause trouble if a diode detector were to be used.

A broadband amplifier with 102dB gain is a likely candidate for stability problems. The three-stage strip used in this receiver is less liable to power supply feedback than most since the SL612C has internal supply decoupling. Nevertheless it must be carefully laid out to minimise earth loops and input/output feedback. The simplest way to do this is to use a double-sided printed circuit board with the components side a continuous ground plane to which all earth connections are made. If this is done the layout on the conductor side of the board is not very critical but if single-sided board is used with the earth conductors on the same side as the other conductors then it does become so. The design of board in Fig. 20 is the most stable layout yet developed for such strips on single-sided board, and it is strongly recommended that it be copied exactly.

There are two other possible causes of instability in this transceiver: inadequate supply switching and inadequate supply decoupling. Since the only on-board transmit/receive switching is by means of power switching it is essential that the transmit supply be not only isolated but earthed during receive, and vice versa. Both supplies should also be well decoupled at RF.

The IF strip has AGC applied to it by an SL621C audio AGC circuit, IC8. AGC is applied via an emitter follower, which has the effect of reducing the AGC range of each SL612C by 0.7V. The overall AGC range could be reduced to less than 90dB were only two SL612Cs to have AGC applied to them. AGC is therefore applied to all three to give 130dB, of which the usable AGC range is about 115dB.

The IF output is applied to an SL640C double-balanced modulator (IC6), used here as a product detector. When AGC is operating, the audio output of

the detector is about 10mV RMS. The audio is fed to IC7, an SL630C audio amplifier which has a voltage gain control. The SL630C can supply up to about 60mW to headphones, to a small loudspeaker or to an external amplifier.

The detected audio also goes to the SL621C audio AGC system (IC8). This has an ideal characteristic for SSB reception. It operates from the receiver audio, not from RF, and it has fast attack and fast decay unless a signal disappears altogether — as in speech pauses — when it does not decay at all for a second and then, if the signal has not reappeared, decays quickly. This enables it to track rising or fading signals but prevents it overloading after each brief speech pause. The circuit also incorporates very fast AGC action to suppress brief noise bursts.

An FET oscillator is used to supply carrier to the product detector and to the double-balanced modulator in the transmitter. The voltage applied to the 'sideband select' terminal determines which crystal is used — upper or lower sideband — but the terminal must not be left unconnected: it must either be connected to +6V or to earth. The oscillator is supplied via diodes from both the transmit and receive lines so that it continues to operate on transmit or receive.

The most basic receiver does not have an 'S' meter but if one is required it may be connected to the emitter of the AGC buffer transistor. It should consist of a moving coil meter connected in series with a resistor such that FSD corresponds to 2.5V and three forwardbiased silicon diodes. This 'S' Meter circuit has a rather compressed scale for signals more than 40dB above the AGC threshold.

This receiver has a sensitivity of 1.0 microvolts for 10dB S/N. This means that at HF with adequate antennas no RF amplifier is required since atmospheric noise will limit system performance. At higher frequencies, or in systems where small antennas are used, RF gain may be necessary to prevent the performance being gain-limited rather than noise limited. Such amplifiers increase gain but degrade intermodulation performance. In general, without the RF amplifier, the receiver will tolerate about 200mV of adjacent channel signal on the mixer without significant intermodulation. This is, of course, a property of the mixer rather than of the rest of the circuit, although the filter characteristics are also involved.

The Transmitter

The transmitter uses the standard filter method of generating SSB. Audio from the microphone is fed to an SL622C microphone amplifier (IC9), which has AGC giving a constant 100mV output over 60dB of input. The AGC ensures an almost constant output from the transmitter, but can be inconvenient in noisy environments when the transmitter will give full modulation on noise in the absence of a speech input. Such noise modulation is avoided by the addition of a single extra resistor (R5, between pins 8 and 9 of the SL622C) which reduces the dynamic range of the AGC.

The constant-level audio from IC9 is applied to the signal input of an SL640C double-balanced modulator (IC5). The output of the FET carrier oscillator is applied to the carrier input of IC5 and a double sideband suppressed carrier signal appears at its output. Carrier suppression is of the order of 40dB.

This DSB signal is amplified in an SL610C (ICl). The AGC pin of ICl is brought out from the board and may be used either to preset the system gain or as an ALC connection. The amplified DSB from IC1 is then passed through

the crystal filter, which removes one sideband, leaving SSB. The SSB is mixed to the final transmitter frequency in the diode ring mixer and then goes to a linear amplifier which raises it to the transmitter output level. The output from the diode ring is, of course. lower than the input to the filter and is about 100mV or less into 50 ohms.

The output of IC5 and the input of the first SL612C (IC2) are connected to the same point on the filter via resistors. R6 is merely a buffer resistor but R2 and R1 set the impedance which the filter sees in operation. This varies from 480 ohms on transmit to about 530 ohms on receive, but this small variation does not affect filter performance. The loading effects of a turned-off SL612C during transmission and a turned-off SL610C during reception are similarly insignificant.

The transmitter output (at the diode ring) consists of an SSB signal with carrier below — 55dB and opposite sideband below — 60dB, provided that the carrier oscillator is at the correct frequency. The degree of off-channel spurious signals depends on the crystal filter used: 90dB stopband type gives excellent performance but a cheaper one can sometimes cause trouble.

The Transceiver

The transceiver board needs few extra sub-systems to make a complete transceiver. They are: a power supply, microphone, volume control and loudspeaker and also a filter, local oscillator and linear amplifier. These are connected as shown in Fig. 21.

Much of the performance of the final system will depend upon the standard of design of the local oscillator, pre-selector, RF amplifier (if used) and linear amplifier, but the performance of the transceiver board itself is excellent. The Anzac MD-108 mixer used is capable of the required performance between 10kHz and 500MHz. If other diode rings were used the transceiver might be used over an even wider range. Its power consumption is about 400mW on either transmit or receive.

The most attractive feature of this transceiver, despite its high performance, is its simplicity. It uses only 80 components and contains no tuned circuits or other components requiring adjustment. It was designed for two purposes: (a) to demonstrate the usefulness and versatility of the SL600 Series in SSB applications and (b) as a ready-engineered SSB transceiver suitable for those inexperienced in SSB design. It is capable of giving good performance but can be constructed and commissioned by relatively inexperienced personnel.

Physical Construction

The board and component layouts are shown in Fig. 20. The board is single-sided and there are two jumper links on it carrying power supplies. As mentioned above the layout on a single-sided board carrying such a high gain broadband IF strip is critical and it should not be changed. All passive component leads should be as short as possible and integrated circuits should not be mounted more than 6mm above the board.

The two transformers T1 and T2 are both wound on small toroids of high frequency ferrite. The exact size and material are not important but the material must be low loss up to at least 45MHz and it is essential that it has a linear B/H characteristic, otherwise it will cause intermodulation at the receiver

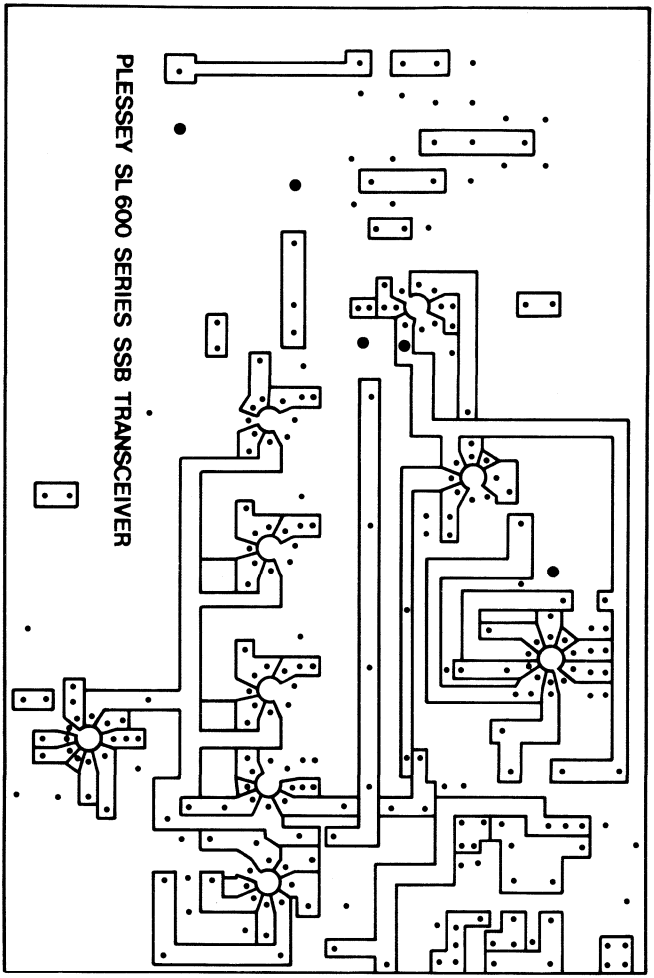


Fig. 20a Copper side of PCB for simple SSB transceiver

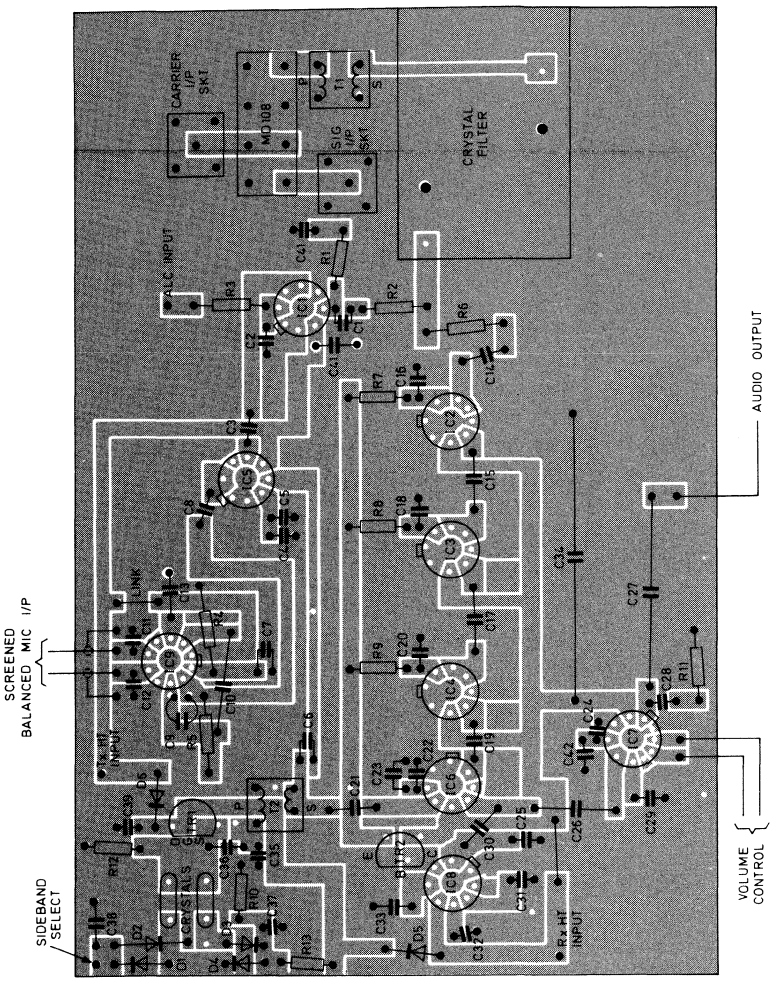


Fig. 20b PCB for simple SSB transceiver

input. T2 is a simple transformer with a six-turn primary and a single turn secondary but T1 is more complex. T1 is made from four 5cm lengths of 26 SWG (0.46mm dia.) enamelled copper wire twisted together. The length of twist is used to wind two turns on the toroid and the ends are separated. Three lengths are then connected in series in the same sense to form the filter winding and the last length is used as the diode ring winding.

There are few other constructional details that need mentioning, but if a receiver without a transmitter is required one may be built by omitting the three transmitting integrated circuits (SL610C, SL622C and the SL640C) between them), R1 to R5 inclusive and C1 to C13 and C40. To preserve the filter impedance match a 500 ohm resistor should be connected from the filter side of R6 to earth.

Component	Value	Rating	Type
R1	100	1/8 W	Hi-Stab.
R2	430	1/8 W	Hi-Stab.
R3	100	1/8 W	Hi-Stab.
R4	680K	1/8 W	Hi-Stab.
R5	1K	1/8 W	Hi-Stab.
R6	50	1/8 W	Hi-Stab.
R7-R9	100	1/8 W	Hi-Stab.
R10	330	1/8 W	Hi-Stab.
R11	10	1/8 W	Hi-Stab.
R12	100K	1/8 W	Hi-Stab.
R13	330	1/8 W	Hi-Stab.
D1-D6			1N4148 } Or similar
TR1			2N3819 } devices
TR2			2N706 }
T1, T2	See text.		
Mixer	Anzac MD-108		
Crystals	9.0015 MHz & 8.9985 MHz		Parallel (30p) resonant
IC1	SL610C		
IC2-IC4	SL612C		
IC5-IC6	SL640C		
IC7	SL630C		
IC8	SL621C		
IC9	SL622C, SL6270C		
C1-C4	1nF	50V	Weecon (Min Ceramic)
C5	10µF	6.3V	Min. Tantalum
C6	100pF	50	Ceramic
C7	47µF	6.3V	Min. Tantalum
C8	10µF	6.3V	Min. Tantalum
C9	4.7nF	50V	Weecon
C10	2µF	6.3V	Min. Tantalum
C11-C12	1nF	50V	Weecon
C13	100nF	50V	Weecon
C14-C15	100pF	50V	Ceramic
C16	4.7nF	50V	Weecon

Table 1 Components list for the Simple SSB Transceiver (Fig. 19)

Component	Value	Rating	Type
C17	100pF	50V	Ceramic
C18	4.7nF	50V	Weecon
C19	100pF	50V	Ceramic
C20	4.7nF	50V	Weecon
C21	100pF	50V	Ceramic
C22	1nF	50V	Weecon
C23	10µF	6.3V	Min. Tantalum
C24	4.7nF	50V	Weecon
C25	100nF	50V	Weecon
C26	10µF	6.3V	Min. Tantalum
C27	100µF	6.3V	Min. Tantalum
C28	10nF	50V	Weecon
C29	1nF	50V	Weecon
C30	1µF	6.3V	Min. Tantalum
C31	100µF	6.3V	Min. Tantalum
C32	47µF	6.3V	Min. Tantalum
C33	100µF	6.3V	Min. Tantalum
C34	400µF	16V	Min. Al. Elect.
C35-C36	68pF	50V	Ceramic
C37-C38	10nF	50V	Weecon
C39-C41	100nF	50V	Weecon
C42	100pF	50V	Ceramic

Table 1 (continued)

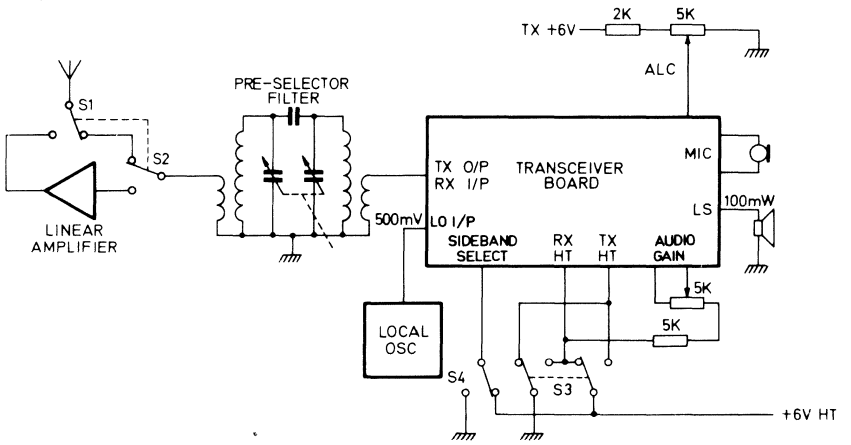


Fig. 21 Block diagram of complete SSB transceiver

Introduction to SL6000 Series

The Plessey Semiconductors SL6000 series of radio linear circuits extends the concept of the 'building block' approach to wider systems. Each device features advanced circuit techniques which result in higher levels of integration, lower power consumption or exceptional performance. All products are available in plastic and metal can or ceramic packages.

SL6000 PRODUCT RANGE (AS AT 1st AUGUST 1979)	
IF AMPLIFIERS/DETECTORS	
SL6600	FM Double Conversion with PLL Detector
SL6640	FM Single Conversion, audio stage (10.7MHz)
SL6650	FM Single Conversion (10.7MHz)
SL6690	FM Single Conversion, low power for pagers (455kHz)
SL6700*	AM Double Conversion
AUDIO	
SL6270*	Microphone Amplifier with AGC to give 'constant' output
SL6290*	SL6270 plus speech clipper, buffer and relay driver
SL6310*	Switchable audio amplifier (400mW/9V/8ohms)

* in development

SL6600C

LOW POWER IF/AF PLL CIRCUIT FOR NARROW BAND FM

The SL6600 is a single or double conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits the SL6600 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with a second IF frequency of less than 1MHz. Normally the SL6600 will be fed with a first IF signal of 10.7 or 21.4MHz; there is a crystal oscillator and mixer for conversion to the second IF amplifier, a PLL detector and squelch system.

IF Amplifiers and Mixer

The SL6600 can be operated either as a single conversion circuit with a maximum recommended input frequency of 800kHz or in a double conversion mode with a first IF of the input frequency (50MHz max.) and a second IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IFs; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 25 MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used.

When a single conversion circuit is required a 6.8k resistor should be connected in place of the crystal and a further 2.7k resistor connected between pin 1 and earth. The overall gain of the circuit will be reduced by 12dB with this technique.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz.

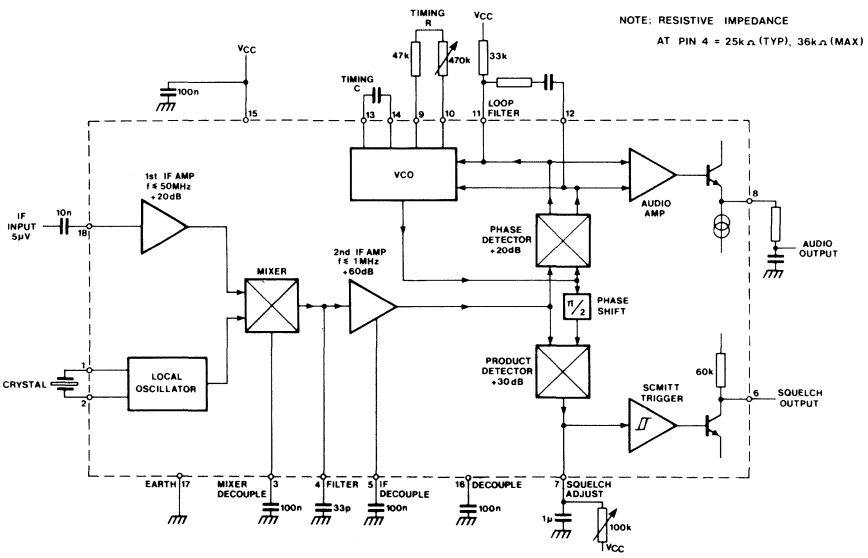


Fig. 22 SL6600 Block diagram

Phase Locked Loop.

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor according to the formula (30/f)pF where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine +10% frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 47k (recommended minimum value) increases the frequency by approx. 10%.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be calculated so that the natural loop frequency fn and damping factor ξ are suitable for the FM deviation and modulation bandwidth required. Values of 6.2k and 2.2nF are recommended for ±5kHz maximum deviation and 3kHz audio bandwidth when the second IF frequency is 100kHz. These give fn = 20kHz ξ = 0.707.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. This feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7k and 4.7nF may be used.

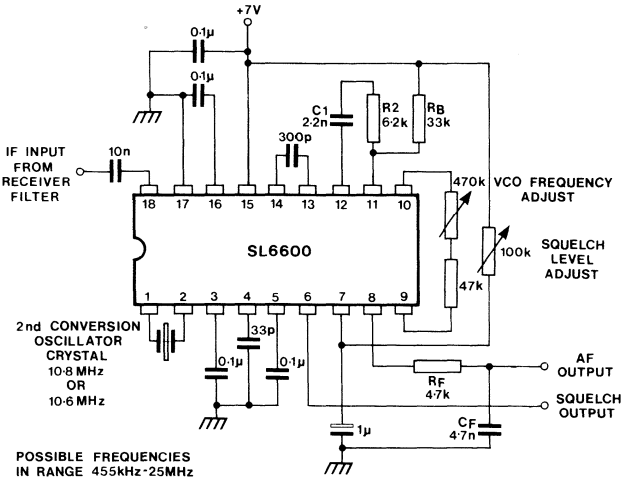
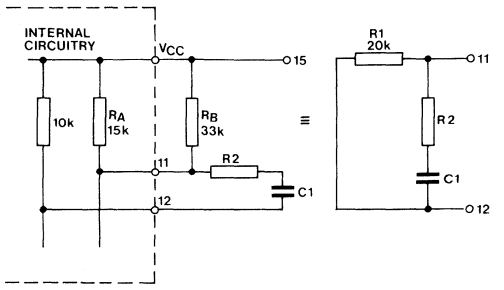


Fig. 23 SL6600 application diagram (1st IF=10.7MHz, 2nd IF=100 kHz)

LOOP FILTER DESIGN

The design of the loop filter determines the allowable deviation of the received FM, the bandwidth of the modulating audio and the signal-to-noise ratio which may be achieved. With wide-deviation signals the filter may be omitted altogether and the system will work perfectly well, but with a somewhat reduced signal-to-noise ratio which is nevertheless quite acceptable in many applications. The filter (Fig.24) consists of a resistor and capacitor (R2 and C1) in series between pins 11 and 12. The external 30 kΩ resistor mentioned above produces a composite resistor, R1, of 20 kΩ formed by the series connection of the two resistors on the chip and the external resistor in parallel with one of them.



$$2\pi f_n = \left(\frac{K_o K_D}{\tau_1 + \tau_2}\right)^{\frac{1}{2}}$$

$$= \frac{1}{2}\left(\frac{K_o K_D}{\tau_1 + \tau_2}\right)^{\frac{1}{2}}\left(\tau_2 + \frac{1}{K_o K_D}\right)$$

Fig. 24 SL6600 loop filter circuit

The loop constants of the SL6600 are:–

K_O = 2.4f_O Radians/Volt second
K_D = 2.8 Volts/Radian
R1 = 20k Ω
$K_O K_D$ = 6.7f_O sec^{-1}

Other variables used in driving the loop filter are:–

f_O The VCO centre frequency
Δf The peak deviation
f_n The natural frequency of the loop
f_m The maximum modulation frequency
ϕe The maximum phase error in the loop
ξ The damping Factor

The values of f_m and Δf are part of the system specification and together with f_O specify ϕe. The VCO centre frequency is generally chosen to be 100kHz or 10Δf, whichever is the greater. Maximum frequency is 1MHz. The damping factor, ξ, is usually chosen to be 0.707. Fig.25 shows the relationship between ϕe, f_m and Δf for ξ = 0.707.

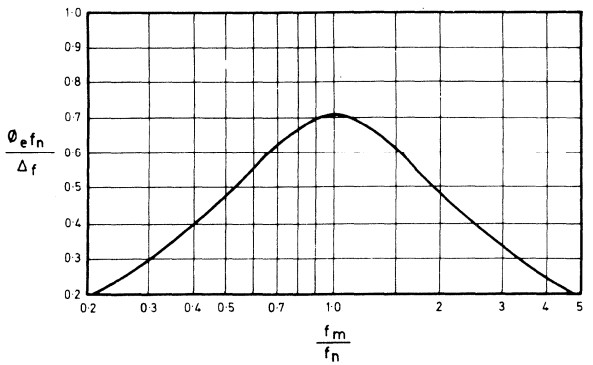


Fig. 25 Phase error for damping factor = 0.707

EXAMPLE $\Delta f = 5kHz; f_m = 3kHz, f_o = 100kHz$

$$\text{Therefore } \phi_e \max = \frac{0.93\Delta f}{f_o} = \frac{0.93 \times 5 \times 10^3}{100 \times 10^3} = 0.046 \text{ radians}$$

The problem now is to deduce the value of f_n from Fig. 4; this is an iterative process.

(i) Put $f_n = 10kHz$. Therefore $\frac{f_m}{f_n} = \frac{3}{10} = 0.3$

from Fig. 4 $\phi_e = \frac{0.3 \times 5 \times 10^3}{10 \times 10^3} = 0.15$ radians (too large)

(ii) Put $f_n = 20kHz$. Therefore $\frac{f_m}{f_n} = \frac{3}{20} = 0.15$

from Fig. 4 $\phi_e = \frac{0.17 \times 5 \times 10^3}{20 \times 10^3} = 0.043$ radians,

which agrees closely with the required value. Knowing the natural frequency the loop time constants can now be evaluated:–

$$t_1 + t_2 = \frac{K_O K_D}{(2\pi f_n)^2} = \frac{6.77 \times 10^3}{(2 \times \pi \times 20 \times 10^3)^2} = 42.9\mu s$$

$$t_2 = \frac{2D}{2\pi f_n} = \frac{0.707}{\pi \times 20 \times 10^3} = 11.2\mu s$$

$$t_1 = 31.7\mu s \; C = \frac{t_1}{R_1} = 1.6nF$$

$$R_2 = \frac{t_2}{C} = 7k\Omega$$

SL6640 and SL6650

for single conversion receivers with quadrature detectors

The SL6640 and SL6650 are illustrated in Fig.26. Each consists of an IF limiting preamplifier, a main limiting amplifier, a quadrature detector, a squelch system, and a DC audio gain control. In addition, the SL6640 contains a low-power audio output stage.

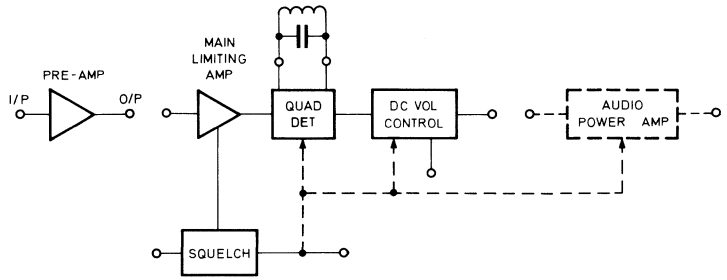


Fig. 26 Block of SL6640 and SL6650 (broken line applies to SL6640 Only)

The IF preamplifier has a bandwidth of 25 MHz, a gain of about 46 dB (200 times), and an input impedance of 5 kΩ shunted by 2 pF. It consists of five cascaded long-tailed pairs and has excellent limiting characteristics.

The main IF amplifier also has a bandwidth of 25 MHz but its gain before limiting is about 60 dB (1000) and it consists of six long-tailed pairs. The third and sixth of these stages contain detectors, the outputs of which drive the squelch system. The output of the limiting amplifier feeds a double-balanced modulator and also an external phase-shift circuit which in turn feeds the other port of the double-balanced modulator. This double-balanced modulator thus acts as a quadrature detector. The quadrature detector in the SL6640 and SL6650 has very good performance when demodulating narrow band FM signals, even when working with intermediate frequencies of up to 21.4 MHz. This is because at over 50 kΩ, the impedance of the quadrature port is high and so the Q of the quadrature circuit is not impaired by being loaded, as is so often the case with integrated circuit quadrature detectors.

The external phase shift circuit is fed via internal capacitors of only 2 pF and so the quadrature circuit works well only at about 4.5MHz and above. The SL6640 and SL6650 cannot, therefore, be used at the common 455kHz IF. The SL6690 (see below) works very well at this frequency, however, and should be used when 455kHz operation is required.

The audio output from the quadrature circuit goes to an audio amplifier which is DC-controlled to allow the use of remote gain control. The output of the SL6650 is taken from this gain control, but the SL6640 has an extra audio amplifier capable of driving a small 8Ω loudspeaker.

The squelch system is driven by the detectors in the IF strip and contains a comparator which requires an input to set the squelch level. A resistor between

this programming input and the squelch output provides hysteresis to the system. In the SL6650 the squelch system merely provides a DC output to indicate the presence of a signal larger than the squelch threshold but in the SL6640 the squelch controls the power supply to both the detector and the audio stages. The standby power of the SL6640 is thus the lower even though it is the more complex circuit.

The SL6640 is manufactured in an 18 lead DIL package and the SL6650 in a 16 lead DIL. The devices are designed so that as many as possible of their pins are common i.e., pins 1 to 6 are identical and pins 13 to 18 of the SL6640 are equivalent to pins 11 to 16 of the SL6650 and only the pins around the audio stages differ. This allows similar board layout to be used in radios using the SL6640 or the SL6650. In the pin-by-pin description which follows, pin numbers are given for the SL6640, those of the SL6650, where they differ, are given in brackets e.g., pin 18 (16).

Pin 1 is the bias point for the main IF amplifier. It must be decoupled effectively by an RF capacitor to ground and connected by a coil or resistor to the IF input, pin 14 (12). If a resistor is used, it should provide the correct match for the interstage filter; if a coil is used it will probably be part of the filter and must not have any DC connection to ground. The decoupling capacitor must be at least 0.01 μF.

Pin 2 is the squelch programming point and pin 3 the squelch output pin. The squelch level is set by a 470 kΩ variable resistor (which should be increased to 1 MΩ if supplies of over 6V are used) in series with a 47 kΩ resistor between pin 2 and ground. Squelch sensitivity increases with the value of the variable resistor. Pin 3 is at a high potential when no signal is present and drops to near ground potential when a signal is detected. The output current from pin 3 is less than 2 mA but it may, of course, be buffered if necessary.

The decoupling capacitor of 0.33 μF on pin 3 prevents brief breaks in signal (such as mobile flutter) from squelching the circuit. Hysteresis in the squelch is obtained by a resistor connected between pins 2 and 3. The amount of

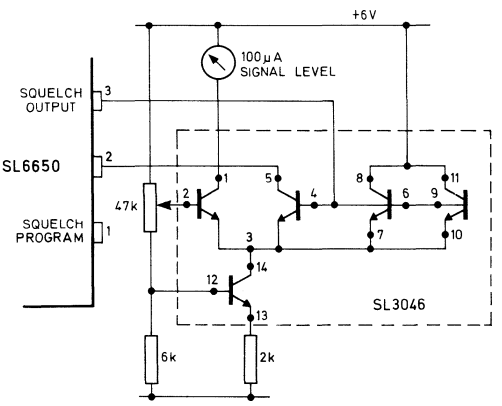


Fig. 27 'S' meter circuit for use with SL6650

hysteresis depends on the squelch threshold, the resistor value and the supply voltage. At 6V supply a 390 kΩ resistor gives 3 to 4 dB hysteresis at 10 μV squelch level and about 10 dB at 100 μV squelch level. Larger resistors are necessary at higher supply voltages and the minimum possible hysteresis rises to about 7 dB with a 1.5 MΩ resistor and a 9 V supply. Despite its variation with supply voltage, the squelch is quite stable with temperature and alters by only 1 to 2 dB as the circuit is temperature cycled. If squelch is not required the SL6650 squelch pins may be used, with an SL3046 transistor array, to drive an S meter as shown in Fig.27. The system consists of a negative feedback amplifier and is not possible with an SL6640, where the internal squelch must always be used.

The quadrature circuit is connected between pins 4 and 5. This can consist of an LC tuned circuit resonant at the centre of the IF passband, or one of the commercial crystal quadrature circuits for NBFM, or even a ceramic interstage filter such as is made for broadcast receiver applications. Ceramic filters usually need to be tuned by a parallel trimmer capacitor and their efficiency as quadrature elements can vary widely from batch to batch. They are not, therefore, the best quadrature elements to choose although they are non-microphonic and smaller than most coils. The resistive element of the impedance between pins 4 and 5 is over 50 kΩ and so has little effect on the Q of a wound quadrature element. Narrow FM can thus be demodulated, even with an LC quadrature element, with an excellent signal-to-noise ratio – 50 dB or better. If a lower Q is required the resistance between the pins may be reduced by the use of an external resistor.

No DC path must exist between pins 4 and 5 and any other point, but they themselves may be connected together if required. It is better to have a DC path between them than not, so long as it is not at the expense of the Q of the quadrature element.

The DC volume control consists of a fixed resistor of 47 kΩ in series with a variable resistor of 470 kΩ connected between pin 6 and ground. The gain range is typically 70 dB (3000:1) and gain is minimum when resistance is minimum.

Pins 12 and 13 of the SL6640 and pin 11 of the SL6650 are the supply pins. SL6640 pin 12 is the audio output stage supply while pin 13 supplies the remainder of the circuit. In the case of the SL6650 pin 11 is the supply connection for the entire circuit. The supply voltage is normally +6V but the circuits will work with supplies between +5V and +9V. Consumption of the SL6640 at 6V is 3.5mA (squelched) and 10mA (unsquelched), or more if audio power is being supplied, while the SL6650 draws 6mA in either case. Pin 12 of an SL6640 may be left unconnected if for any reason the audio stage is not required but it must not be used with more than 0.5V difference in potential between pins 12 and 13.

The power supplies must be well decoupled at RF with at least 0.1μF having low inductance and short leads. The supplies should also have low audio ripple and it is necessary to decouple the SL6640 supply very thoroughly at LF if the audio stage is to operate at its highest powers and retain its AM rejection.

Pin 14 (12) is the input of the main IF amplifier and should be biased by being connected to pin 1 as described above. The input impedance is 5 kΩ shunted by 2 pF.

Pins 15 (13) and 17 (15) are decoupling points within the circuit and should be decoupled to earth by good RF capacitors, preferably 0.1 μF and at least 0.01 μF. Inadequate decoupling of these pins causes poor AM rejection and can cause instability.

Bias circuitry for both the main amplifier and the preamplifier is shown in Fig.28. The preamplifier input is pin 16 (14). It is not self biased but is fed with bias from pin 18 (16) via a total of about 15 kΩ. The input impedance of the preamplifier is 5 kΩ shunted by 2 pF. If, as is common, the preamplifier is fed from a filter requiring a precise match, the value of resistor R2 should be chosen to provide this. The source impedance driving the preamplifier should be 750 Ω or less to prevent instability. The input signal should be fed to pin 16 (14) via a capacitor or other DC block. The sum of resistors R1 and R2 should be 15 kΩ and their junction well decoupled at HF. The noise figure of the preamplifier is 7 dB when driven by 350 Ω.

The preamplifier output is pin 18 (16) and it has an output impedance of 300 Ω. Signal is taken from the output of the preamplifier to the input of the

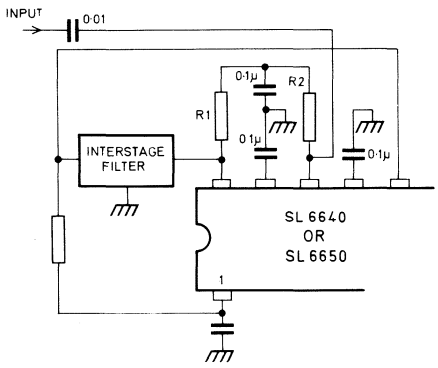


Fig. 28 Bias circuit for SL6640 and SL6650

main amplifier via an interstage filter. This is a roofing filter to provide some limitation of noise bandwidth, not the primary selectivity of the receiver which must be provided by a high performance filter placed before the preamplifier. This filter, therefore, need have neither a good shape factor nor large stop-band attenuation. Any simple filter is suitable but at 10.7 MHz, cheap ceramic filters are particularly useful since they are small and require no setting-up. Much work with the SL6640 and SL6650 has used Murata SFE 10.7 MA filters since they match the output impedance of the preamplifier.

The final part of this section deals with those pins whose functions differ between the SL6640 and the SL6650. First the SL6640. Pin 7 is the output of the DC controlled audio preamplifier and is an emitter follower with a low current tail. It will only drive high impedance loads and needs an HF rolloff capacitor to earth of $\frac{0.01\ \mu F}{f}$ where f is the desired rolloff frequency in kHz.

In normal use pin 7 is connected to pin 8, the input to the output stage, by a 0.1 μF capacitor. Pin 8 is biased by connecting it to the centre of two 220 kΩ resistors connected between the positive supply and ground, in series.

Pin 9 of the SL6640 is the inverting input to the output stage and is used to provide negative feedback to define both DC operating point and stage gain. The feedback resistor from the output pin 11 is 120 kΩ and the gain-defining resistor (which is connected from pin 9 to ground via an isolating capacitor of 1 μF) can be any value greater than 1.2 kΩ. The gain is equal to the ratio of these two resistors, and hence when the smaller is 1.2 kΩ the gain is 40 dB (100). Attempts to achieve higher gain leads to instability and, more important, excessive distortion since the open loop gain of the output stage is only some 55 dB.

Pin 10 is earth and pin 11 is the audio power output. Pin 11 is decoupled to earth with 0.22 μF to ensure HF stability and drives its load via a 100 μF capacitor. With care, and a 9V supply, the SL6640 will drive an 8Ω loudspeaker at 250mW but a more practical figure is around 175mW. A complete circuit diagram of an SL6640 in use is shown in Fig.29.

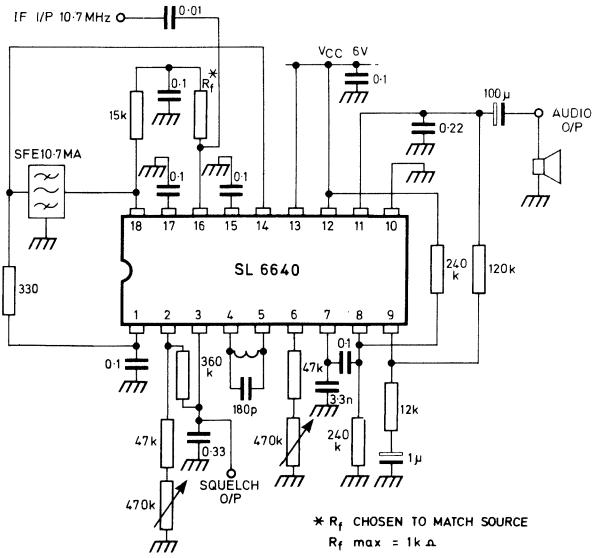


Fig. 29 10.7MHz application of SL6640

Pins 7 and 9 of the SL6650 are unused. Pin 8 of the SL6650 is earth and pin 10 is the audio output. This output appears on the open collector of a transistor and so must be connected to the positive supply by a resistor – generally 10kΩ. Audio is taken through a capacitor and the pin is also decoupled at HF.

by a capacitor of $\frac{0.015\ \mu F}{f}$ where f is the cutoff frequency in kHz.

SL6690

ultra-low power consumption quadrature detector system

The SL6690 block diagram is shown in Fig. 30. The circuit consists of a limiting IF amplifier which drives a quadrature detector, an LF amplifier and Schmitt trigger (which can be used either as a signal-to-noise squelch system or as a squarer when the circuit is used in a pager), and a voltage regulator which uses an external PNP transistor.

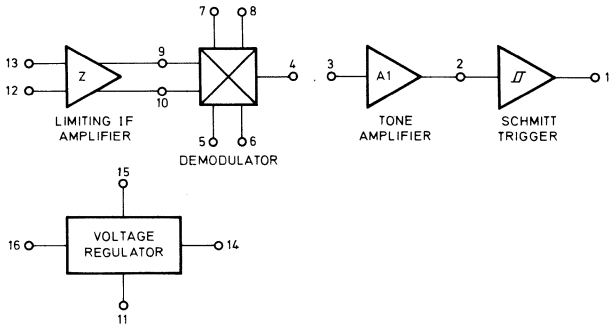


Fig. 30 SL6690 block diagram

The IF amplifier has a bandwidth of 1.5 MHz, making the circuit particularly useful at the popular communications and paging IF of 455 KHz. Its input impedance is 20 kΩ shunted by 2 pF and its output impedance is about 2 kΩ. Bias is obtained by DC feedback from the outputs to the inputs.

The quadrature detector is a conventional double-balanced modulator using transistor tree techniques. The quadrature circuit is an external LC tuned circuit and the capacitors driving the quadrature circuit are also external, which allows the detector to be used down to VLF as well as up to about 1.5 MHz.

The LF amplifier has a gain of 54 dB and is biased by a DC connection from its output to its input. It is an inverting amplifier so its gain and frequency characteristics may be defined by negative feedback. The Schmitt trigger is driven directly by the LF amplifier. Its output is a free collector which may be connected to either V_{CC} (the regulated supply) or the unregulated supply rail. In its ON state it will sink up to 150 μA.

The regulator, which requires an external series PNP transistor, allows the SL6690 to work from supplies between +2.5 and +6V. The external transistor is necessary because monolithic PNP transistors have poor h_{fe} at very low current levels.

Pin 1 is the Schmitt trigger output, a free collector which can sink up to 150 μA when the transistor is turned on and can rise to either V_{CC} or some other positive rail up to +6V when turned off. The input to the Schmitt trigger and the output of the LF amplifier are connected internally and the node brought out to pin 2. Bias must be taken from this pin to the LF amplifier input, pin 3,

via a resistance of 50 kΩ or less. The LF amplifier inverts and its gain and passband may be defined by negative feedback. An output may be taken from pin 2 and the Schmitt trigger left unused in which case no connection need be made to pin 1. The bias of the amplifier/Schmitt combination is sufficiently accurate to give the Schmitt an output mark-space ratio of between 0.9:1 and 1.1:1 with a sine wave input to the amplifier. The LF amplifier input impedance is 50 kΩ and its open loop gain roughly 54 dB.

No DC connections should be made from pin 3 except the bias connection to pin 2; all inputs should be coupled via capacitors. To prevent HF instability 2.2 kΩ in series with 120 pF should be connected from pin 2 to ground.

The output of the quadrature detector is pin 4 and its output impedance is 1 kΩ. The detector will give an output of 10 mV/Degree phase change and distortion of about 3 per cent (more if a ceramic resonator is used as a quadrature element). A single filter capacitor removes RF from the detected output.

The quadrature circuit is connected between pins 5 and 6 and may be a parallel tuned LC circuit or a ceramic resonator. The port has an input impedance of 50 kΩ shunted by 2 pF. The quadrature circuit may or may not present a DC path between the two pins. Use of ceramic quadrature elements usually results in greater distortion than the use of LC elements but such ceramic elements occupy less space and do not require adjustment. The quadrature circuit is driven by the output from pins 7 and 8 via two capacitors. Pin 7 drives pin 5 and pin 8 drives pin 6. The value of the capacitors depends on the frequency of operation and the quadrature circuit used.

Pins 9 and 10 are the outputs of the IF amplifier and are used to provide bias to its inputs. A 100 kΩ resistor is connected from pin 10 to pin 12 and pin 12 is grounded at AC by a capacitor. Pin 9 is connected to pin 13, the signal input pin, by another 100 kΩ resistor in series with a resistor of the correct value to terminate the IF source. The junction of the two resistors is decoupled at RF by a low inductance capacitor. The IF input is applied to pin 13 from the IF filter, via a coupling capacitor if necessary to isolate pin 13 at DC.

Pin 11 is earth and pins 14, 15, and 16 the supply/regulator pins. The supply, which may be between 2.5V and 6V is applied to pin 16 and to the emitter of a high gain PNP transistor whose base is connected to pin 15 and collector to pin 14. Pin 14 is stabilised at 2V and must be thoroughly decoupled at RF by a 0.1μF capacitor. The SL6690 may be turned on in 12 milliseconds or less so the power supply may be strobed in paging applications so that the mean power dissipation in the circuit is an order of magnitude lower than its normal 2mW (1mA @ 2V).

FM RECEIVERS USING SL6000 SERIES

The SL6600, SL6640, SL6650 and SL6690 are intended for use in NBFM receivers – mobile, hand-portable, base station and paging. They are all intended for use as IF Amplifier/Detector/Squelch modules and, of course, the SL6640 has a low power audio output stage.

The circuits, having low power consumption and, indeed, limiting amplifiers, have low resistance to intermodulation (although they have excellent dynamic range) and must be used after the main selectivity of the receiver. Modern receiver design emphasises strong signal performance even at the expense of sensitivity and hence front ends having much gain are not popular. This can

leave an uncomfortable gap between the 2 to 4 μV output from a receiver filter and the 10 μV or so that these circuits require to give an adequate signal-to-noise ratio. Redesign of the front end to give slightly more gain is possible and certainly the easiest solution but it may produce an unacceptable reduction in intermodulation performance. An amplifier is therefore needed between the filter and the SL6600/40/50/90.

This amplifier can be a convenience (some filters have matching impedances so high that even the input impedances of these circuits are embarassingly low) but, preceeding as it does a very high gain integrated circuit, it can suffer from stubborn instability. It also increases the power consumption of the receiver which is annoying in a hand-portable, although a hand-portable with its limited antenna is most likely to be able to tolerate a higher gain front end and hence least likely to need an extra stage of IF gain.

Suitable amplifiers may be made with a single transistor or FET and two circuits are shown in Fig.31. The FET circuit uses more current and an FET with a good performance at 1 mA and a low pinch-off voltage is required. The transistor circuit is far less demanding but has a lower input impedance (which depends on h_{fe} and C_{ob} and will vary from device to device). These amplifiers must be very well isolated if the receiver is to be stable and the powerful decoupling of the transistor circuit is a point in its favour.

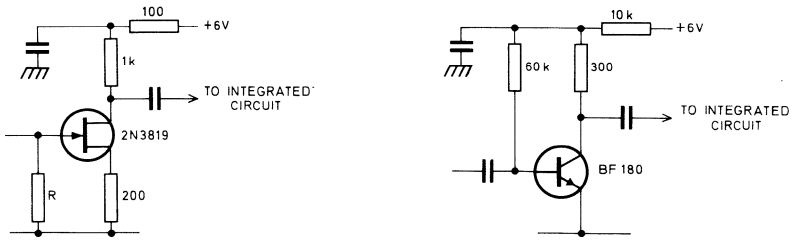


Fig. 31 FET and bipolar buffer amplifier

Apart from the occasional necessity for a low-gain preamplifier these circuits present few problems and are very easy to use. As mentioned above, some attention must be paid to layout to isolate input and output, particularly at the same frequency, as much as possible. Other points to be remembered are the use of non-inductive capacitors (many capacitors are inductive at frequencies as low as 5 MHz) and adequate decoupling of all bias points and power supplies – in connection with this it is worth remembering that it is useless to use a good RF capacitor with short leads if the printed connection to it is long and narrow.

It is not intended to describe in detail the design of any complete receivers using these circuits. However, a review of the various types of receiver where these circuits may be used and the considerations affecting such use is given below.

LAND MOBILE RADIOS

In the VHF or UHF bands land mobiles use narrow deviation FM (between 1.5 and 12kHzΔf) and generally use a first IF of 10.7 or 21.4MHz. Transceivers can be hand-held or vehicle mounted. For hand-held transceivers the choice is between the SL6600 which has low power consumption and can be strobed and the SL6640 which has an integral output stage. The signal-to-noise ratio of either circuit is adequate when used with the recommended circuitry but there is a performance difference. The capture effect of a PLL detector is much better than that of a quadrature detector: a receiver using an SL6600 will capture the stronger of two co-channel signals even if it is only stronger by 2 to 4dB. The SL6640 will be affected by a co-channel interfering signal until it is 20dB or more below the wanted signal. Both features can be valuable; some (including military) users need to know of other signals on-channel while others, particularly in areas where channels are shared with space diversity, prefer systems which ignore low-level co-channel interference.

An advantage of the SL6640 is that it has only one conversion, saving a crystal (although the crystal used with the SL6600 need not be expensive since the main selectivity of the receiver preceeds the SL6600 and slight frequency drift in the second crystal oscillator will not move the signal out of the detector or squelch passband) and eliminating the possibility of 'birdies' from a second oscillator. Most manufacturers' quadrature detectors, having been designed primarily for TV use, require a low IF if they are to give an adequate signal-to-noise ratio at low deviations but the SL6640 and SL6650 are capable of giving over 50dB signal-to-noise ratio with deviations as low as 1.5kHz at an IF of 10.7MHz.

In land mobile applications with FM deviations in the range 1.5 to 12kHz the SL6600 is used with a second IF of 100kHz. The design of the loop filter depends on the deviation and audio bandwidth (generally 3kHz for speech) as mentioned above. The double conversion can ease problems of instability if it is necessary to use an amplifier between the quartz filter and the SL6600 since the total gain of the first IF is not so high.

PAGING RECEIVERS

Using the SL6690 a paging receiver can run on only two cells and consumes only 2 mW, which may be further reduced to as little as 100μW if the receiver is strobed. Such pagers are small, simple, inexpensive, and use few components.

BROADCAST F.M. RECEIVERS AND TV SOUND IF SYSTEMS

These can use the SL6640/50 merely by using a quadrature element with lower Q to accommodate the wider deviation. The circuit alteration can be as simple as the addition of a resistor between pins 4 and 5 to load the quadrature coil, although the main selectivity of the receiver must be suitable for the bandwidth of the new type of signal. The SL6640 is especially useful in portable FM receivers in that it will supply adequate power to a loudspeaker but consumes only a few milliamps, porlonging battery life.

The SL6600 is less suitable for broadcast applications, although it works very well when it is used with a second IF around 800kHz and gives particularly low distortion due to its PLL detector. Its disadvantage is the cost of the crystal in the second converter although this is not too great and might be overcome by the use of a series resonant LC tuned circuit.

OTHER APPLICATIONS

These circuits can be used in various applications, including microwave and telemetry receivers and, with the SL6640/50, simple SSB receivers requiring very low power.

The choice of circuit in any application depends on a number of factors including deviation and type of modulation. In general, providing the shift is not too great, the SL6600 is better for RF FSK, although the loop filter design requirements will differ from those described above when the modulation departs so far from sinusoidal. On the other hand the SL6640/50 will cope with deviations of 2 to 3MHz providing an IF of twenty-odd MHz is used and the quadrature element has low enough Q.

Using the SL6640/50 as an SSB receiver involves replacing the quadrature circuit with a BFO so that the detector works as a product detector, and applying the AGC, preferably audio-derived with an SL621 or similar system, to an amplifier preceeding the SL6640/50 to prevent its IF amplifier from limiting.

Section 2
High Speed Dividers

Introduction to SP8000 series

The SP8000 Series is a range of high speed digital dividers using ECL techniques. Devices with division ratios from ÷2 to ÷256 are available and some types operate at frequencies up to 1.5GHz. To describe the various types in full is outside the scope of this book. However, since high speed dividers have numerous applications in radio systems, a brief description of the range and some notes on applications for the circuits will be given.

SP8000 PRODUCT RANGE

Divide by	Product	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Control input		Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	TTL	ECL	Metal can	Ceramic	Plastic
3/4	SP8720A	●				300		●			40		●		●		●	
5/6	SP8692A	●				200	●				14	●	●	●	●		●	
	SP8692B				●	200	●				14	●	●	●	●		●	
	SP8740A	●				300		●			45		●		●		●	
	SP8740B				●	300		●			45		●		●		●	
6/7	SP8741A	●				300		●			45		●		●		●	
	SP8741B				●	300		●			45		●		●		●	
8/9	SP8691A	●				200	●				14	●	●	●	●		●	
	SP8691B				●	200	●				14	●	●	●	●		●	
	SP8743A	●				500		●			45	●	●		●		●	
	SP8743B				●	500		●			45	●	●		●		●	
10/11	SP8690A	●				200	●				14	●	●	●	●		●	
	SP8690B				●	200	●				14	●	●	●	●		●	
	SP8647A	●				250	●	●			50		●	●	●		●	
	SP8647B				●	250	●	●			50		●	●	●		●	
	SP8643A	●				350	●	●			50		●		●		●	
	SP8685A	●				500		●			45	●	●		●		●	
	SP8685B				●	500		●			45	●	●		●		●	
	SP8680A	●				600		●			90	●	●	●	●		●	
	SP8680B				●	600		●			90	●	●	●	●		●	
20/22	SP8785M		●			1000		●			85		●		●		●	
	SP8785B				●	1000		●			85		●		●		●	
	SP8786M		●			1300		●			85		●		●		●	
	SP8786B				●	1300		●			85		●		●		●	

Table 2 Two-Modulus SP8000 series high speed dividers

Divide by	Product	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	Metal can	Ceramic	Plastic
2	SP8604A	●				300		●			12		●	●		
	SP8604B				●	300		●			12		●	●		
	SP8602A	●				500		●			12		●	●		
	SP8602B				●	500		●			12		●	●		
	SP8607A	●				600		●			14		●	●		
	SP8607B				●	600		●			14		●	●		
	SP8605M		●			1000		●			70		●		●	
	SP8605B				●	1000		●			70		●		●	
	SP8608M		●			1000			●		70		●		●	
	SP8608B				●	1000			●		70		●		●	
	SP8606M		●			1300		●			70		●		●	
	SP8606B				●	1300		●			70		●		●	
	SP8609M		●			1300			●		70		●		●	
	SP8609B				●	1300			●		70		●		●	
4	SP8790A	●				60	●	●			8	●		●		
	SP8790B				●	60	●	●			8	●		●		
	SP8601A	●				150		●			18	●	●	●		
	SP8601B				●	150		●			18	●	●	●		
	SP8600A	●				250		●			16	●	●	●		
	SP8600B				●	250		●			16	●	●	●		
	SP8610M		●			1000		●			70		●		●	
	SP8610B				●	1000		●			70		●		●	
	SP8617M		●			1300			●		80		●		●	
	SP8617B				●	1300			●		80		●		●	
	SP8611M		●			1500		●			70		●		●	
	SP8611B				●	1500		●			70		●		●	
	SP8619M		●			1500			●		80		●		●	
	SP8619B				●	1500			●		80		●		●	
5	SP8620A	●				400		●			55		●		●	
	SP8620B				●	400		●			55		●		●	
8	SP8794A	●				120	●	●			10	●		●		
	SP8794B				●	120	●	●			10	●		●		
	SP8670A	●				600		●			45		●		●	
	SP8670B				●	600		●			45		●		●	
	SP8735B				●	600		●			70	Ⓑ	●		●	
	SP8677M		●			1200			●		70		●		●	
	SP8677B				●	1200			●		70		●		●	

Table 3 Fixed-Modulus SP8000 high speed dividers

Divide by	Product	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	Metal can	Ceramic	Plastic
10	SP8660A	●				200	●	●			10	●		●		
	SP8660B				●	200	●	●			10	●		●		
	SP8660			●		200	●	●			10	●				●
	SP8632B				●	400		●			70		●		●	
	SP8637B				●	400		●			75	ⓑ	●		●	
	SP8630A	●				600		●			70		●		●	
	SP8630B				●	600		●			70		●		●	
	SP8635B				●	600		●			75	ⓑ	●		●	
	SP8634B				●	700		●			75	ⓑ	●		●	
	SP8665B				●	1000			●		80		●		●	
	SP8667B				●	1200			●		80		●		●	
16	SP8659A	●				200	●	●			10	●		●		
	SP8659B				●	200	●	●			10	●		●		
	SP8650A	●				600		●			45		●		●	
	SP8650B				●	600		●			45		●		●	
20	SP8657A	●				200	●	●			10	●		●		
	SP8657B				●	200	●	●			10	●		●		
	SP8658			●		200	●				20	●				●
24	SP8656			●		200	●				20	●				●
32	SP8655A	●				200	●	●			10	●		●		
	SP8655B				●	200	●	●			10	●		●		
64	SP8755A	●				1200	●				45	●			●	
	SP8755B				●	1200	●				45	●			●	
	SP8750B				●	1000			●		68	●			●	
	SP8752M		●			1200			●		68	●			●	
80	SP8627			●		150	●	●			33	●				●
100	SP8628			●		150	●	●			33	●				●
	SP8629			●		150	●	●			33	●				●

Table 3 *(continued)*

CIRCUIT DESCRIPTIONS

Table 3 summarises the SP8000 range of fixed modulus dividers (i.e. those which divide by a single ratio) and Table 2 summarises the two-modulus programmable dividers (i.e. those dividing by N or N + 1 depending on the state of a control input). It will be seen that there are a wide number of division ratios and input/output interfaces but all the devices in the SP8000 range use emitter coupled logic (ECL) chip circuitry.

The signal inputs of SP8000 devices can be differential or single-ended and DC or AC coupled depending on the particular device. Signal is supplied to AC coupled devices via an isolating capacitor (usually about 1000pF) but DC coupled devices have no internal bias circuitry and may be driven either from ECL II or ECL III or be driven with AC via a capacitor and biased by a separate external resistor network.

The datasheet for each device states which of the two ECL families is appropriate and also describes the bias network. Devices with balanced inputs may be driven with a differential signal, or a single signal may be applied to one input and the other decoupled to ground by a 1000pF capacitor.

If no signal is applied to a balanced input the device will tend to oscillate at some ill-defined but high frequency. This may be prevented by applying a bias to one of the inputs by means of a resistor connected from the input to one or other of the supplies. This has the effect of desensitising the input but preventing oscillation – the exact value of the resistor depends on the device used but is generally around 10 kilohms. SP8000 series devices will operate with sinewave inputs at high frequencies but low frequency sine inputs may cause malfunction.

Dividers specified to have maximum operating frequencies of 700 MHz or more should not be used with sine inputs under 80MHz. At frequencies lower than this they should be driven with square wave inputs having rise and fall rates in excess of 200V/microsecond. Lower frequency dividers may be used with sine inputs down to 40MHz and then with square waves with 100 microsecond rise and fall times. Some SP8000 circuits are less demanding – details are given in their respective data sheets.

The input signal required by SP8000 series circuits for satisfactory operation is between 400 and 800mV peak-to-peak except in the case of one or two of the very high speed dividers which require a minimum of 600mV. Many dividers will operate with inputs well outside this range but it is unwise to allow them to do so as the circuit configurations used in the counters can lead to miscounting at certain frequencies if too high or too low an input level is used.

The control inputs of the two-modulus dividers are ECL-compatible.

The majority of SP8000 outputs are emitter followers, usually ECL-compatible, but some of the series have free collector or TTL compatible outputs. Many of the devices have both Q and $\overline{Q}$ and some of the decades have BCD outputs.

No particular problems arise in the output circuitry although the emitter follower outputs should not be used to drive capacitivie loads.

The SP8000 series circuits require 5.2V supplies except a few of the faster circuits, which require higher voltages such as 6.8V or 7.4V. The data sheets suggest the use of positive ground supplies; this has the advantage of minimising the risk of damage due to output short circuits but can be inconvenient if the dividers are to be used in conjunction with other integrated

circuits using the more conventional negative ground. But whether positive or negative ground is used it is most important that the power supplies be adequately decoupled. Quite small capacitors may be used — 100pF is more than ample and in some applications as little as 15pF has been shown to be sufficient.

The capacitors used must, however, be RF types having minimal lead and package inductance. The capacitors should be sited as close to the integrated circuits as possible and leads kept short. It is not use ensuring that a capacitor lead is short if the printed track to it is long and thin — board tracks must also be kept short and as wide as possible. A ground plane on one side of the circuit board with all ground connections made to it minimises lead inductance problems and is the best way to ensure satisfactory operation of any high speed or high frequency circuitry.

Similar care to that spent on decoupling should be lavished on the bias points in the circuit and the unused inputs. Capacitors need not be particularly large but must have good high frequency performances and very short leads and tracks.

MODULUS EXTENDERS FOR TWO-MODULUS DIVIDERS THE SP8790 AND SP8794

The SP8790 and the SP8794 are designed for use with two-modulus dividers to extend their division ratios and hence make them more suitable for use with CMOS and low power TTL. The SP8790 converts a $\div N/N+1$ counter to a $\div 4N/4N+1$ counter and the SP8794 converts it into a $\div 8N/8N+1$ counter.

Each device consists of a counter with a balanced AC-coupled input, a CMOS or TTL compatible output, and a control output designed to drive the control inputs of the SP8000 series of two-modulus dividers. There is also a control input which is CMOS or TTL compatible (but needs a 5 kilohm pullup resistor when used with TTL).

In use, the control input from the programmable divider goes to the control input of the SP8790 (or the SP8794) and is gated to the two-modulus divider once every four (or eight) counts. Fig. 32 shows an SP8790 used with an SP8690 to give a $\div 40/41$ counter; similar systems may be used with any of the SP8000 two-modulus dividers.

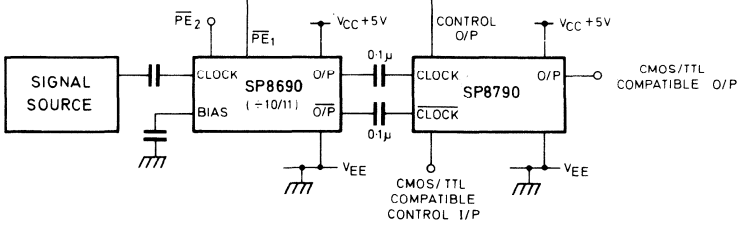


Fig. 32 SP8790 with SP8690 to give a ÷40/41

The SP8790 and SP8794 will normally be driven by SP8000 high speed dividers which have fast output edges. If other sources are used, however, the notes on input waveform slew rate in the preceding section should be observed. Again, the input should be biased if there is likelihood of instability in the absence of a signal, and the unused input should be decoupled to ground if only one input is required. The input level should be between 300mV and 1V peak-to-peak.

The internal delays in the SP8790 and the SP8794 do not allow their operation at input frequencies (to the SP8790 or SP8794) of over 40MHz as a controller. However, if the SP8790 or SP8794 are used as simple dividers they will work at over 60MHz and 120MHz respectively.

Both devices require a single 5V supply which must, as usual, be well decoupled. Neither device has any other points which need to be decoupled with the possible exception of unused inputs.

Input characterisation for the SP8000 series

Because of the wide frequency range of the SP8000 series emitter-coupled logic dividers, the input drive and impedance should be optimized.

The input impedance from 50MHz to 600MHz is mostly capacitive. Beyond 600MHz it becomes inductive.

To optimize the circuit to handle large overloads, small signals, and changes of input impedance versus operating frequency some suggestions are offered in Figs.33, 34 and 35.

Where the frequency range to be used covers an impedance change of greater than three to one, a circuit shown in Fig. 33 could be added to the input. By using the appropriate input impedance curve and calculating the value of R & L, the total input impedance would be more constant over the required frequency range.

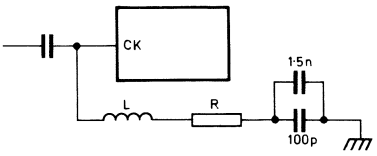


Fig. 33

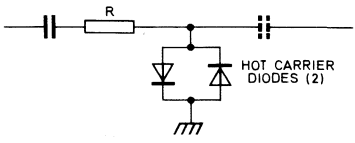


Fig. 34

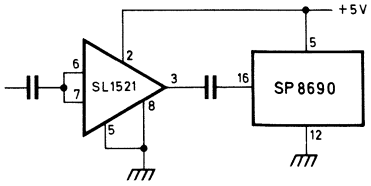


Fig. 35

In the case of large overloads the circuit shown in Fig. 34 could be used.

When using this circuit there is typically a 3dB loss in sensitivity but the dynamic range would be increased from two to one to over four to one. The value of R depends on the maximum overdrive voltage and the hot carrier diodes used.

For low level inputs an SL1521 wideband amplifier could be used as a preamplifier for a divider as shown in Fig. 35.

By using the SL1521 and the SP8690 low power 200MHz divide by 10/11 divider, as shown in Fig. 35, the minimum sensitivity is reduced from 143mV RMS to 36mV RMS. Both units are self biased and require only coupling capacitors for interconnections. Also both parts operate from the same +5V supply at 145mW total power.

When using the SP8600 series it is recommended that good low inductance RF capacitors be used on all bias and power supply decoupling points.

The printed circuit board should be laid out with all input leads as short as possible, ample ground plane around the device and using other normal RF techniques.

SP8602,4,7

INPUT IMPEDANCE

The input impedance is shown in Fig.36 for the frequency range of 50MHz to 700MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.1pF.

TEST CIRCUIT

The test circuit is shown in Fig.37. All tests were made at 25°C.

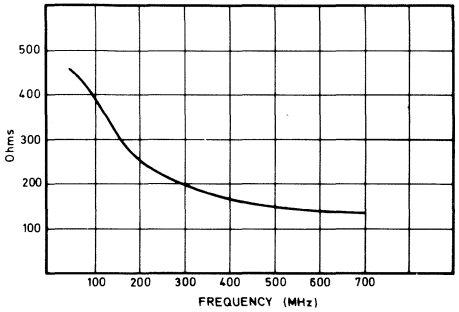


Fig. 36

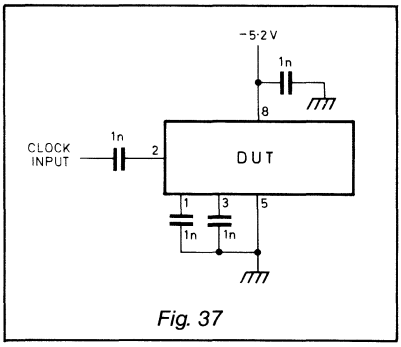


Fig. 37

SP8630,2

INPUT IMPEDANCE

The input impedance is shown in Fig.38 for the frequency range of 50MHz to 600MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.9F.

TEST CIRCUIT

The test circuit is shown in Fig. 39. All tests were made at 25°C.

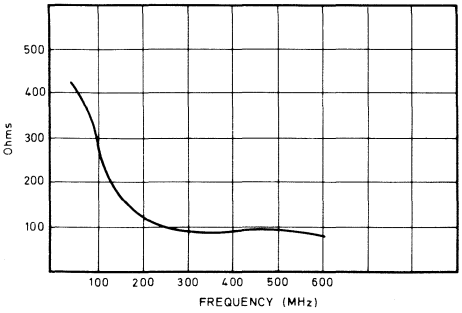


Fig. 38

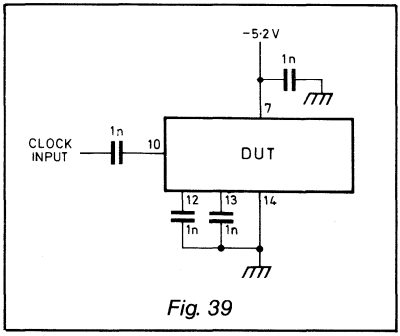


Fig. 39

SP8634,5,7

INPUT IMPEDANCE

The input impedance is shown in Fig. 40 for the frequency range of 50MHz to 700MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 4.1pF.

TEST CIRCUIT

The test circuit is shown in Fig. 41. All tests were made at 25°C.

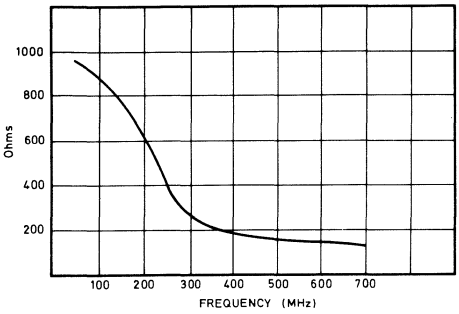


Fig. 40

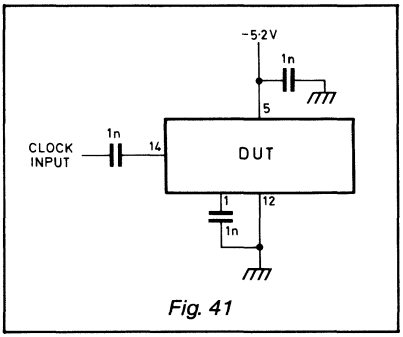


Fig. 41

SP8643,7

INPUT IMPEDANCE

The input impedance is shown in Fig. 42 for the frequency range of 50MHz to 350MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 2.4pF.

TEST CIRCUIT

The test circuit is shown in Fig. 43. All tests were made at 25°C.

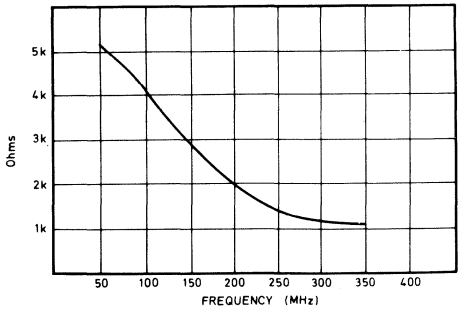


Fig. 42

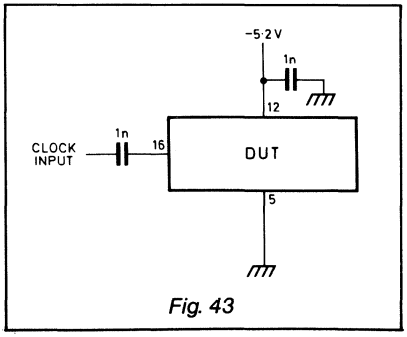


Fig. 43

SP8650

INPUT IMPEDANCE

The input impedance is shown in Fig.44 for the frequency range of 50MHz to 600MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 6.0pF.

TEST CIRCUIT

The test circuit is shown in Fig.45. All tests were made at 25°C.

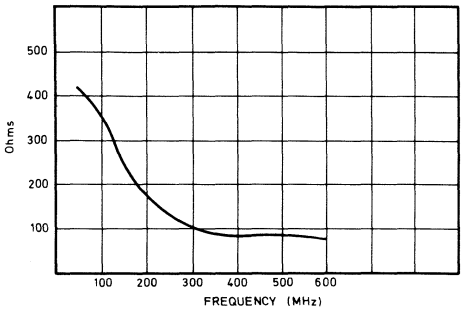


Fig. 44

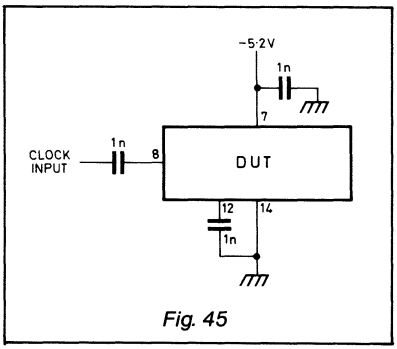


Fig. 45

SP8655,7,9

INPUT IMPEDANCE

The input impedance is shown in Fig.46 for the frequency range of 50MHz to 100MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.6pF.

TEST CIRCUIT

The test circuit is shown in Fig.47. All tests were made at 25°C.

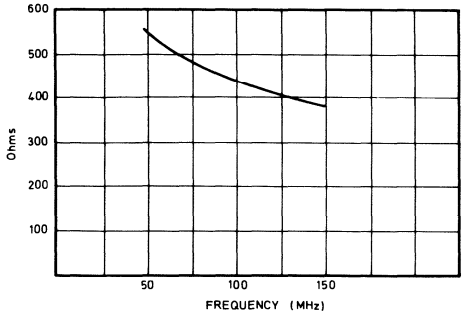


Fig. 46

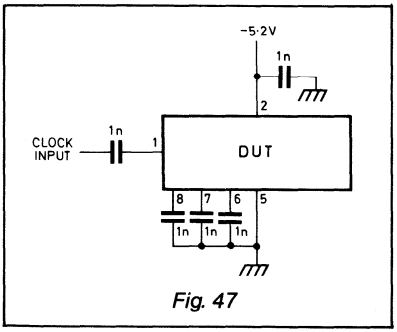


Fig. 47

SP8685

INPUT IMPEDANCE

The input impedance is shown in Fig.48 for the frequency range of 50MHz to 500MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 8.7pF.

TEST CIRCUIT

The test circuit is shown in Fig. 49. All tests were made at 25°C.

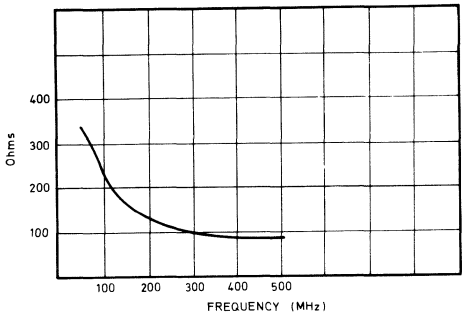


Fig. 48

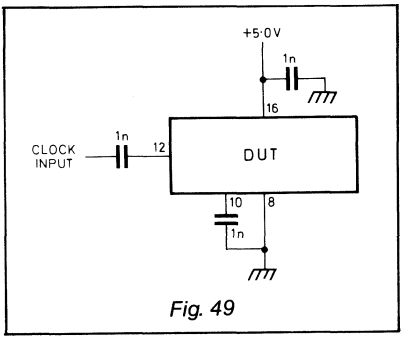


Fig. 49

SP8690

INPUT IMPEDANCE

The input impedance is shown in Fig. 50 for the frequency range of 50MHz to 200MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 6.4pF.

TEST CIRCUIT

The test circuit is shown in Fig. 51. All tests were made at 25°C.

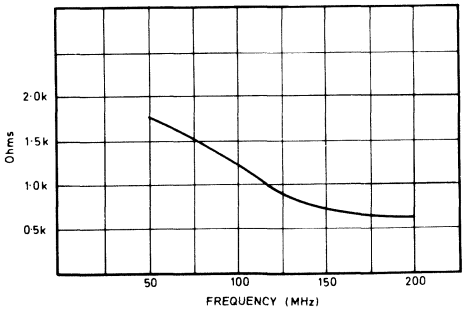


Fig. 50

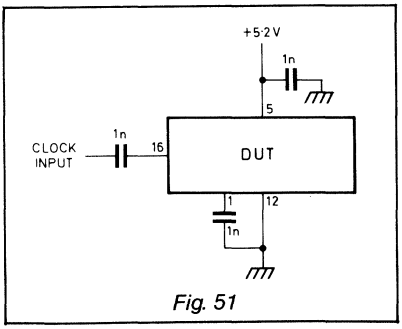


Fig. 51

Preamplifiers for SP8000 series

The availability of low-cost hybrid amplifiers with a performance extending to 1GHz, coupled with SP8000 High Speed Dividers, allows an unparalled increase in instrument performance.

For example, using an Amperex ATF 417 as a preamplifier for an SP8610 (with a Schottky barrier diode limiter), the divider's sensitivity can be improved by at least 15dB. The circuit diagram is shown in Fig.52. Typical room temperature performance is shown in Fig.53, and a suitable PCB layout is given in Fig.54.

Low end performance is limited by signal rise time requirements for the SP8610, whilst high end sensitivity is limited by the amplifier limiter performance. This can be improved by operating the ATF 417 off a higher supply. By increasing the supply to, say, +20V, a gain in sensitivity of, typically, 5dB would be expected at 1GHz.

Similar results can be obtained using the ATF 417 with other dividers such as the SP8667, 1.2GHz decade divider.

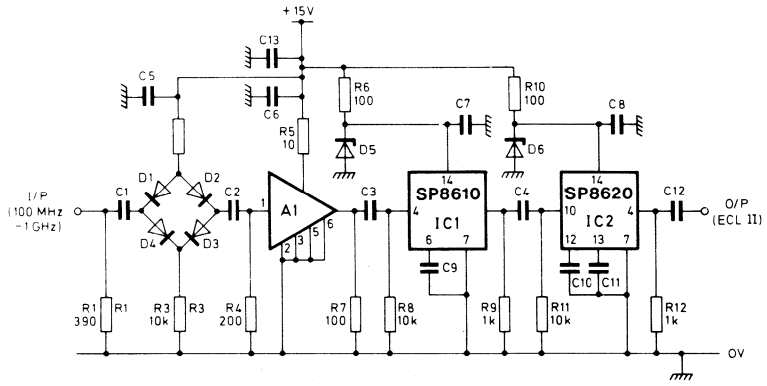


Fig. 52 UHF instrumentation ÷ 20 prescaler

COMPONENTS

D1 – D4	:	Schottky barrier diodes, HP5082–2811
A1	:	Hybrid amplifier, Amperex ATF417 or Philips OM185
IC1	:	Plessey Semiconductors SP8610B
IC2	:	Plessey Semiconductors SP8620B
D5, D6	:	1 Watt, 5.1V Zener diode
R6, R10	:	100 ohms, 5 Watt, e.g. Plessey GWT-5
C1 – C12	:	1nF ceramic, e.g. ITW EMCAPS
C13	:	0.33 microfarad

CIRCUIT DETAILS

The signal input (100MHz–1GHz) is AC-coupled to a Schottky barrier diode bridge which limits at 100mV p/p. The signal is then amplified by the hybrid

A1. This combination gives about 15dB of gain with a supply of 15V. The amplifier is AC coupled, via C3, to an SP8616 ÷4 circuit (IC1). R7 provides an input offset to prevent 'no signal' oscillation. The drive capability of IC1, is increased by R8 and its output capacitively coupled to IC2 via C4 R9 provides the input offset for IC2. The output of IC2 is suitable for driving ECL II.

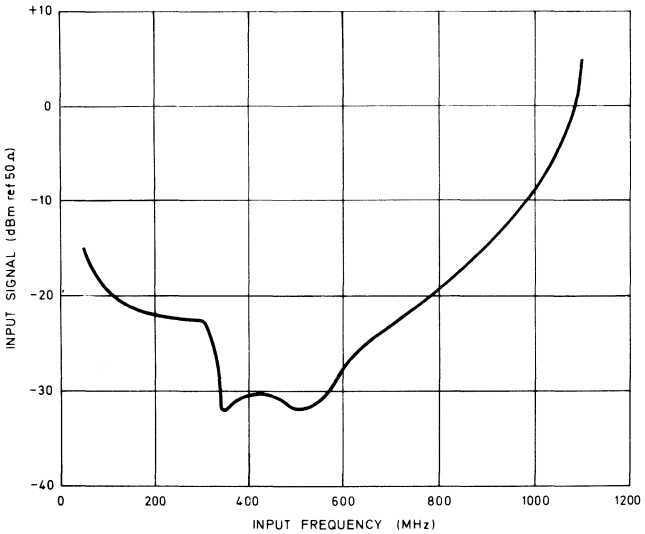


Fig. 53 Typical performance of UHF prescaler

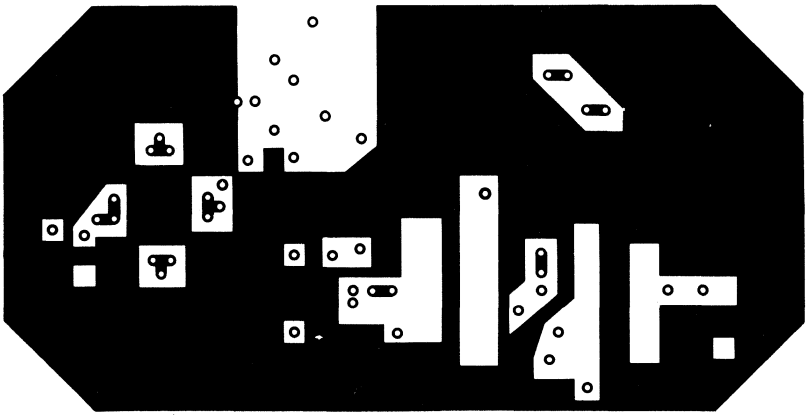


Fig. 54a Component side of board

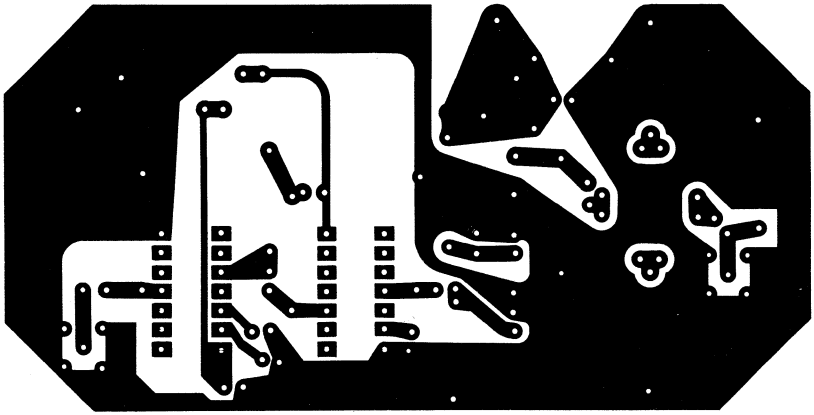


Fig. 54b Solder side of board

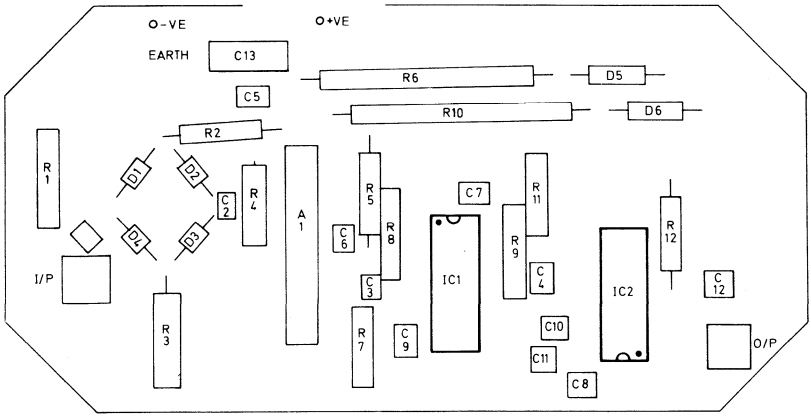


Fig. 54c Component location

Section 3

Synthesiser Circuits

Synthesiser Circuits

INTRODUCTION TO SYNTHESISER SYSTEMS

Fig. 55 shows a typical frequency synthesiser. It consists of a voltage controlled oscillator, a variable divider and a phase comparator. The output frequency of the VCO is a function of an applied control voltage. In frequency synthesisers the function is always monotonic and is generally as near linear as possible.

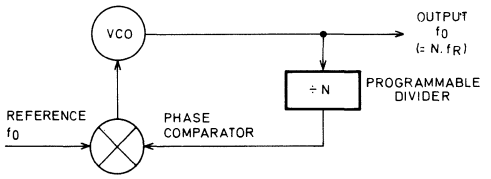


Fig. 55 Basic frequency synthesiser

The output of the phase comparator is a voltage which is proportional to the phase difference between the signals at its two inputs. This output controls the frequency of the VCO so that the phase comparator input from the VCO via the variable divider (÷N) remains in phase with the reference input, f_R, so that the frequencies are equal. The VCO frequency is thus maintained at Nf_R, Such a synthesiser will produce a number of frequencies separated by f_R and is the most basic form of phase locked synthesiser. Its stability is directly governed by the stability of the reference input f_R, although it is also related to noise in the phase detector, noise in any DC amplifier between the phase detector and the VCO and the characteristics of the low-pass filter usually placed between the phase comparator and the VCO.

The design of frequency synthesisers using the above principle involves the design of various sub-systems; including the VCO, the phase comparator any low-pass filters in the feedback path, and the programmable dividers. The following deals mainly with the design of dividers.

PROGRAMMABLE DIVISION

A typical programmable divider is shown in Fig. 56. It consists of three stages with division ratios K_1, K_2 and K_3 which may be programmed by inputs P_1, P_2 and P_3 respectively. Each stage divides by K_n except during the first cycle after the program input P_n is loaded when it divides by P (which may have any integral value from n to K). Hence the counter illustrated divides by $P_3(K_1K_2) + P_2K_1 + P_1$ and when an output pulse occurs the program inputs are reloaded. The counter will divide by any integer between 1 and $(K_1K_2K_3 - 1)$.

The commonest programmable dividers are either decades or divide-by-sixteen counters. These are readily available in various logic families, including CMOS and TTL. It is possible to buy quad decades in CMOS in a single package.

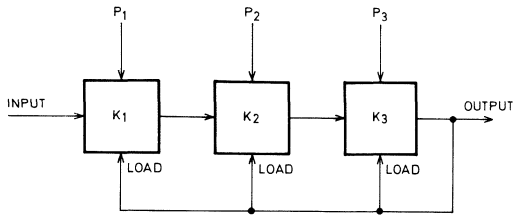


Fig. 56 Typical programmable divider

Using such a package one can program a value of N from about 3 to 9999. The theoretical minimum count of 1 is not possible because of the effects of circuit propagation delays. The use of such counters permits the design of frequency synthesisers which are programmed with decimal thumbwheel switches and use a minimum of components. If a synthesiser is required with less obvious frequencies and steps a custom programmable counter may be made using some custom logic family such as PMOS, NMOS, CMOS or I^2L.

The maximum input frequency of such a programmable counter is limited by the speed of the logic used, and more particularly by the time taken to load the programmed count. Few programmable counters of the type discussed will operate with test frequencies much above 5MHz. The faster types, operating perhaps 25 or 30MHz, use Shottky TTL which consumes considerable power and has a tendency to inject HF and VHF noise into supply lines. The output frequency of the simple synthesiser in Fig. 55 is of course limited to the maximum frequency of the programmable divider.

There are many ways of overcoming this limitation on synthesiser frequency. The VCO output may be mixed with the output of a crystal oscillator and the resulting difference frequency fed to the programmable divider; the VCO output may be multiplied from a low value in the operating range of the programmable divider to the required high output frequency. Alternatively, a fixed ratio divider capable of operating at a high frequency may be interposed between the VCO and the programmable divider. These methods are shown in Figs 57a, 57b and 57c respectively.

All the above methods have their problems although all have been used and will doubtless continue to be used in some applications. Method (a) is the most useful technique since it allows narrower channel spacing or higher reference frequencies (hence faster lock times and less loop-generated jitter) than the other two but it has the drawback that since the crystal oscillator and the mixer are within the loop, any crystal oscillator noise or mixer noise appears in the synthesiser output. Nevertheless, this technique has much to recommend it.

The other two techniques are less useful. Frequency multiplication introduces noise and both techniques must either use a very low reference frequency or rather wide channel spacing. What is needed is a programmable divider which operates at the VCO frequency — one can then discard the techniques described above and synthesise directly at whatever frequency is required.

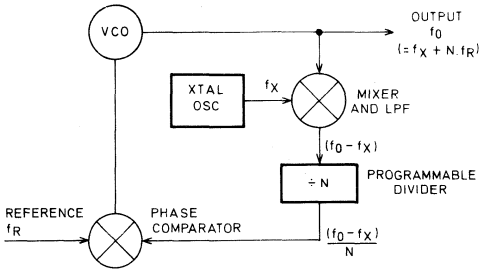


Fig. 57a Mixer synthesiser

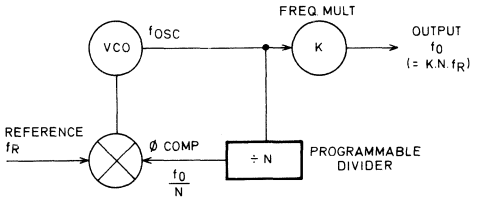


Fig. 57b Synthesiser with ouput multiplication

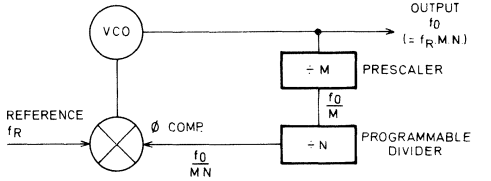


Fig. 57c Synthesiser with prescaler

TWO-MODULUS DIVIDERS

Considerations of speed and power make it impractical to design programmable counters of the type described above, even using ECL, at frequencies much into the VHF band (30 to 300MHz) or above. A different technique exists, however, using two-modulus dividers.

Fig. 58 shows a divider using a two-modulus prescaler. The system is similar to the one shown in Fig. 57c but in this case the prescaler divides either by N or N + I depending on the logic state of the control input. The output of the prescaler feeds two normal programmable counters.

Counters 1 controls the two-modulus prescaler and has division ratio A. Counter 2, which drives the output, has a division ratio M.

In operation the ÷N/N + I prescaler (Fig. 58) divides by N+I until the count in programmable counter 1 reaches A and then divides by N until the count in programmable counter 2 reaches M when both counters are reloaded, a pulse passes to output and the cycle restarts. The division ratio of the whole

system is A(N+1) + N(M—A), which equals NM+A. There is only one constraint on the system — since the two modulus prescaler does not change modulus until counter 1 reaches A the count in counter 2 (M) must never be less than A. This limits the minimum count the system may reach to A(N+1) where A is the maximum possible value of count in counter 1.

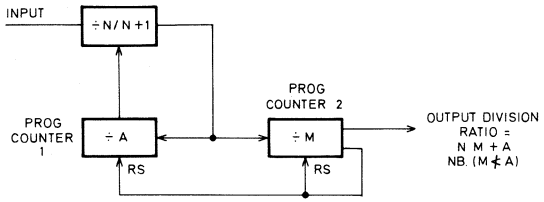
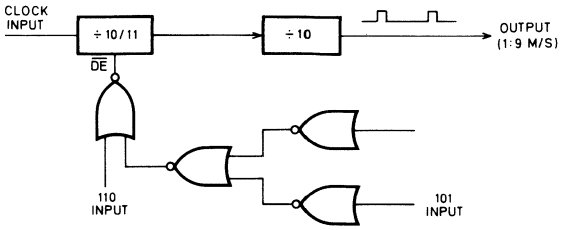


Fig. 58 Divider system with 2 modulus prescaler

The use of this system entirely overcomes the problems of high speed programmable division mentioned above. Plessey Semiconductors make a number of ÷10/11 counters working at frequencies of up to 500MHz and also ÷5/6, ÷6/7 and ÷8/9 counters working up to 500MHz. There is also a pair of circuits intended to allow ÷10/11 counters to be used in ÷40/41 and ÷80/81 counters in 25kHz and 12.5kHz channel VHF synthesisers.
It is not necessary for two-modulus prescalers to divide by N/N+1. The same principles apply to ÷N/N+Q counters where Q is any integer but ÷N/N+1 tends to be most useful.

If the limitation that M must not be less than A is unacceptable the system may be extended to use three or four modulus division. For example if a ÷10/11 prescaler is used in a VHF synthesiser to be programmed in decades the maximum value of A will be 9 and so the minimum frequency will be 99MHz (=A(N+1)). Suppose instead that a ÷100/101/110 counter (which may be made as shown in Fig. 59) is used in the system in Fig. 60. At the start of a cycle the counter divides by 110 until the programmable counter reaches A. This releases the inhibition on programmable counter 2 and the prescaler divides by 101 until counter 2 reaches A_2, at which point the prescaler divides by 100 until counter 3 reaches N and the cycle restarts. The division ratio is therefore $110A_1+101A_2+100(N—A_1—A_2)$ which, by a bit of algebra, is equal to A_2+10A_1+100N.

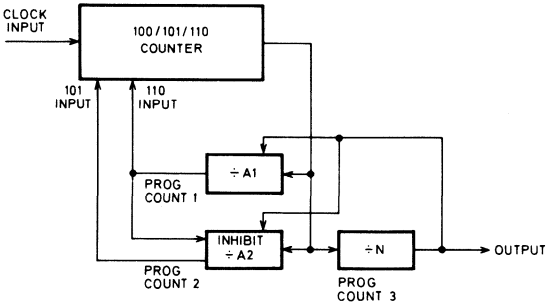
This system allows a minimum count in the programmable counter 3 of A_1+A_2. Since the system is decimal the maximum value of A_1 and A_2 is 9. The minimum value of N is therefore 18 and if the earlier system is replaced with this system it will work down to 18MHz. A similar, but more complex system involving ÷100/101/111 prescaler allows operation down to 10MHz.



LOGIC

INPUT		COUNT
101	110	
L	L	100
H	L	101
L	H	110
H	H	110

Fig. 59 Basic 100/101/110 prescaler



DIVISION RATIO = $A_2 + 10A + 100N$

Fig. 60 Divider system with 100/101/110 prescaler

SYNTHESISER PRODUCT RANGE (AS AT 1st AUGUST 1979)	
CRYSTAL OSCILLATORS	
SP705	1 to 10MHz crystal, outputs at ÷2, ÷4
CRYSTAL OSCILLATORS WITH DIVIDERS	
SP8760	also includes phase comparator
SP8921	also includes part of control circuit
CITIZENS BAND 27MHz PRODUCTS	
SP8921	
SP8922	
SP8923	
UNIVERSAL SYNTHESISER	
SP8901*	4 modulus divider 1GHz
SP8906*	4 modulus divider 500MHz
NJ8811*	Control circuit for use with SP8901 or SP8906
LOWER POWER SYNTHESISER	
NJ8812*	Control circuit for use with ÷40/41 or ÷80/81

* in development

SP705B

CRYSTAL OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: f/2, f/4. $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications.

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig. 62.

The circuit is designed to provide low crystal drive levels — typically, less than 0.15mW at 5MHz. This is well within crystal manufactures' limit of 0.5mW.

The compensation point, pin, 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

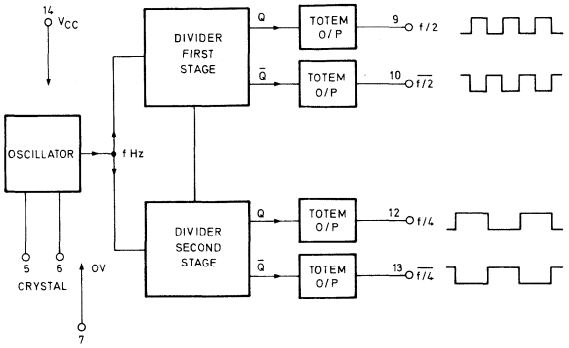


Fig. 61 SP705B block diagram

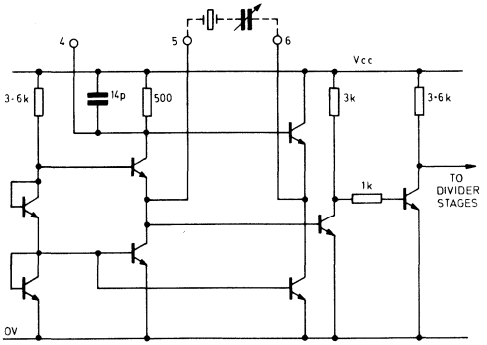


Fig. 62 Circuit diagram of SP705B oscillator

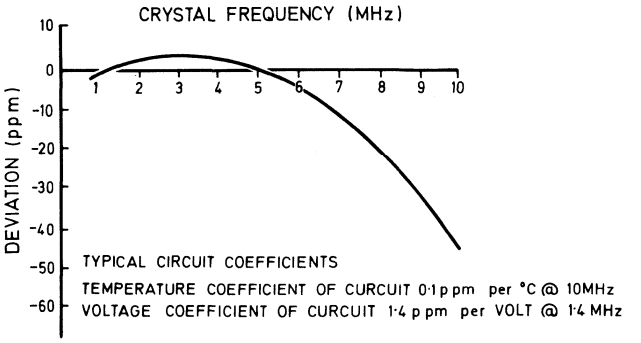


Fig. 63 Deviation from nominal crystal frequency

SP8760

General purpose synthesiser

The SP8760 is a general-purpose circuit intended for use in conjunction with CMOS or TTL programmable counters, and with high speed prescalers, in frequency synthesisers. It consists of a crystal oscillator with two-stage divider, a ÷15/16 two-modulus counter, and a high performance type II phase/frequency comparator. All three sections of the device have CMOS/TTL interfaces and the phase/frequency comparator offers better zero error and phase jitter characteristics than other such integrated circuits.

CIRCUIT DESCRIPTION (Fig.64)

The crystal oscillator uses an emitter-coupled circuit with a series resonant crystal connected between pins 4 and 5. It is internally rolled off to prevent overtone operation and will not work at frequencies much above 10MHz. This oscillator has a series resonant crystal and has a stability of about 0.2ppm/degree C, excluding the crystal itself.

If the divider is required but not the crystal oscillator, an external signal may be applied to pin 4 via a small capacitor in series with 220 ohms. Pin 5 may, in that case, either be decoupled or left open depending on the frequency and amplitude of the signal on pin 4.

The output of the oscillator is not available externally but only via a ÷4 circuit. This circuit, like the rest of the logic interfaces on the SP8760, has a CMOS/TTL compatible output, which is connected to pin 11.

The two-modulus divider (÷15/16) has a CMOS/TTL clock input on pin 6 and its output appears on pin 9. When the control input, pin 8, is high the divider divides by 16 and when it is low it divides by 15. The standard TTL fan-in of the clock input is 1 and the output fan-out is 3.

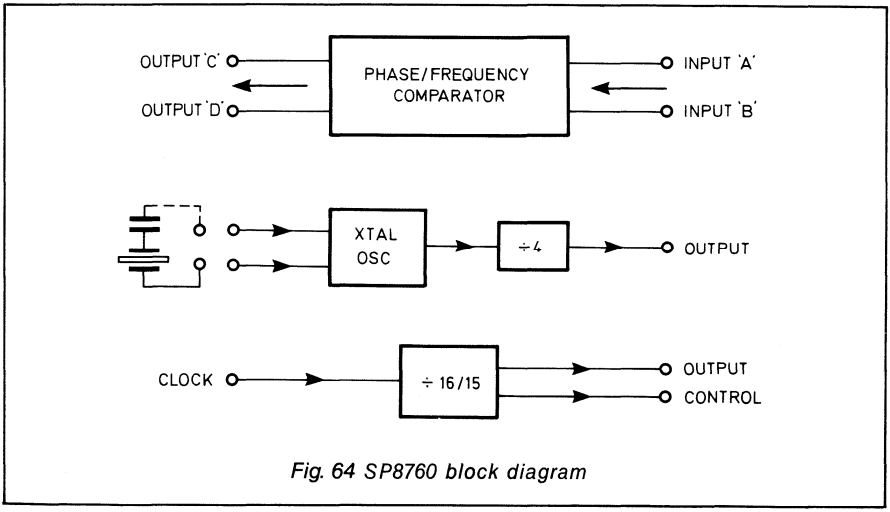


Fig. 64 SP8760 block diagram

The maximum clock frequency of the SP8760 is at least 12MHz (typically 18MHz). Hence the use of almost any family of low speed logic is permissible in the main divider of a synthesiser using the SP8760 since its output will never exceed 1MHz under proper operation.

The comparator has an infinite pull-in range (subject, of course, to an input frequency response of about 10MHz) and zero phase shift at phase-lock. The comparator pulse width at zero phase shift is under 30ns, giving minimum noise and jitter.

In operation the comparator triggers on the 1 to 0 transition of each input and gives outputs on pins 1 and 2 proportional to the phase difference between the two transitions. When the edge on pin 14 occurs before the edge on pin 13 the output on pin 1 will be low during the interval between the two transitions and the output on pin 2 will remain low whereas if the edge on pin 14 occurs after the edge on pin 13 the output on pin 2 will be high between the two transitions and pin 1 will remain high. The decision as to which is the 'first' transition is made by counting pulses at each input — if two pulses occur at one input without any ocurring at the other the second of the two is considered to be the 'first' and the relevant output changes state until a 1 to 0 transition occurs on the other input. Once an input has counted two in this way it remains the 'first' input until two transitions occur on the other input without one ocurring on it, when the other input becomes the 'first' input. The SP8760 phase comparator timing diagram is shown in Fig.65.

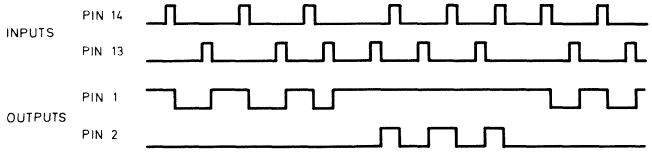


Fig. 65 Phase comparator timing diagram

The output on pin 1 consists of the collector of an NPN transistor with a 10 kilohm resistor to V_{ee}. Three ways of driving the varactor line of a voltage controlled oscillator from these outputs are shown in Fig. 66. The simplest way, shown in Fig. 66(a), is only suitable for use when the varactor voltage change is very small — say, less than 1V from 2 to 3V. The low voltage charge pump in Fig. 66(b) can be used with varactor voltages between 1V and 4V and the high voltage charge pump in Fig. 66(c) is used where large varactor voltage swings are necessary. The transistors and diodes used in these circuits should be silicon types with a fast switching speed to avoid degrading the performance of the phase comparator. The transistors used in the circuit in Fig. 66(c) need also a V_{ceo} of at least 35V.

The leakage on the varactor line must be as low as possible since any leakage leads to jitter as the charge pump replaces the lost charge. A high impedance buffer may be placed between the output of the charge pump and the varactor line and indeed is essential if varactor line losses are high.

Since noise in this buffer will itself cause oscillator jitter, it is better to use a non-leaky varactor line and no buffer if at all possible.

The SP8760 uses a single 5V supply, which must be well decoupled at HF and LF and draw about 45mA.

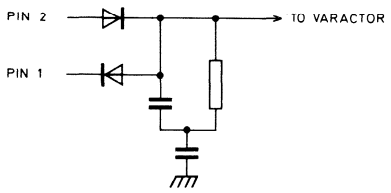


Fig. 66a Simple charge pump

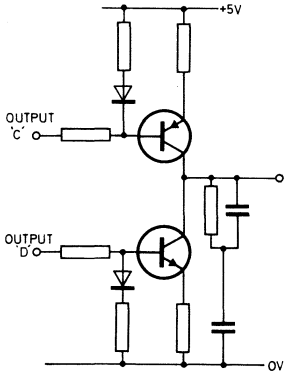


Fig. 66b Low voltage charge pump and filter. Divider clock input

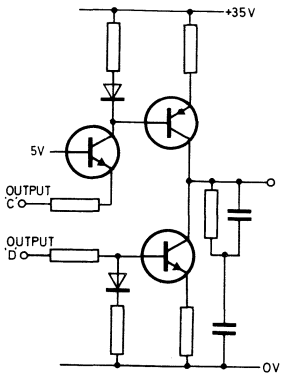


Fig. 66c High voltage charge pump and filter

SP8921/2

CITIZENS' BAND SYNTHESISER

The SP8921/22 combination is intended to synthesise the frequencies required in a 40-Channel Citizens' Band transceiver. The 40 channels are spaced at 10kHz intervals (with some gaps) between 26.965 and 27.405MHz. Local oscillator frequencies for the reception of these channels with intermediate frequencies of 455kHz, 10.240MHz, 10.695MHz and 10.700MHz are also synthesised. Table 4 shows the relationship between the program input and the channel selected. By using a program other than one of the 40 given other frequencies may be selected – in fact there are 64 channels at 10kHz separation available from 26.895 to 27.525MHz and programming starts at all zeros on inputs A through F for 26.895 and each increase of one bit to the binary number on these inputs increases the channel frequency by 10kHz until all '1's give 27.525MHz. The A input is the least significant bit, F the most significant. The programming input on pin 16 of the SP8922 is normally kept high but making it low increases the programmed frequency by 5kHz. Table 5 shows the programming required to obtain various offsets.

The circuit diagram of a CB synthesiser is shown in Fig. 67. It is intended for use in double conversion receivers with IFs of 10.695 and 455kHz and generates either the frequency programmed or the frequency programmed less 10.695MHz.

If other offsets are programmed the connections to pin 15 of the SP8921 and pin 2 of the SP8922 must be altered according to Table 5.

The synthesiser consists of the SP8921 and the SP8922 plus an SP1648 voltage controlled oscillator.

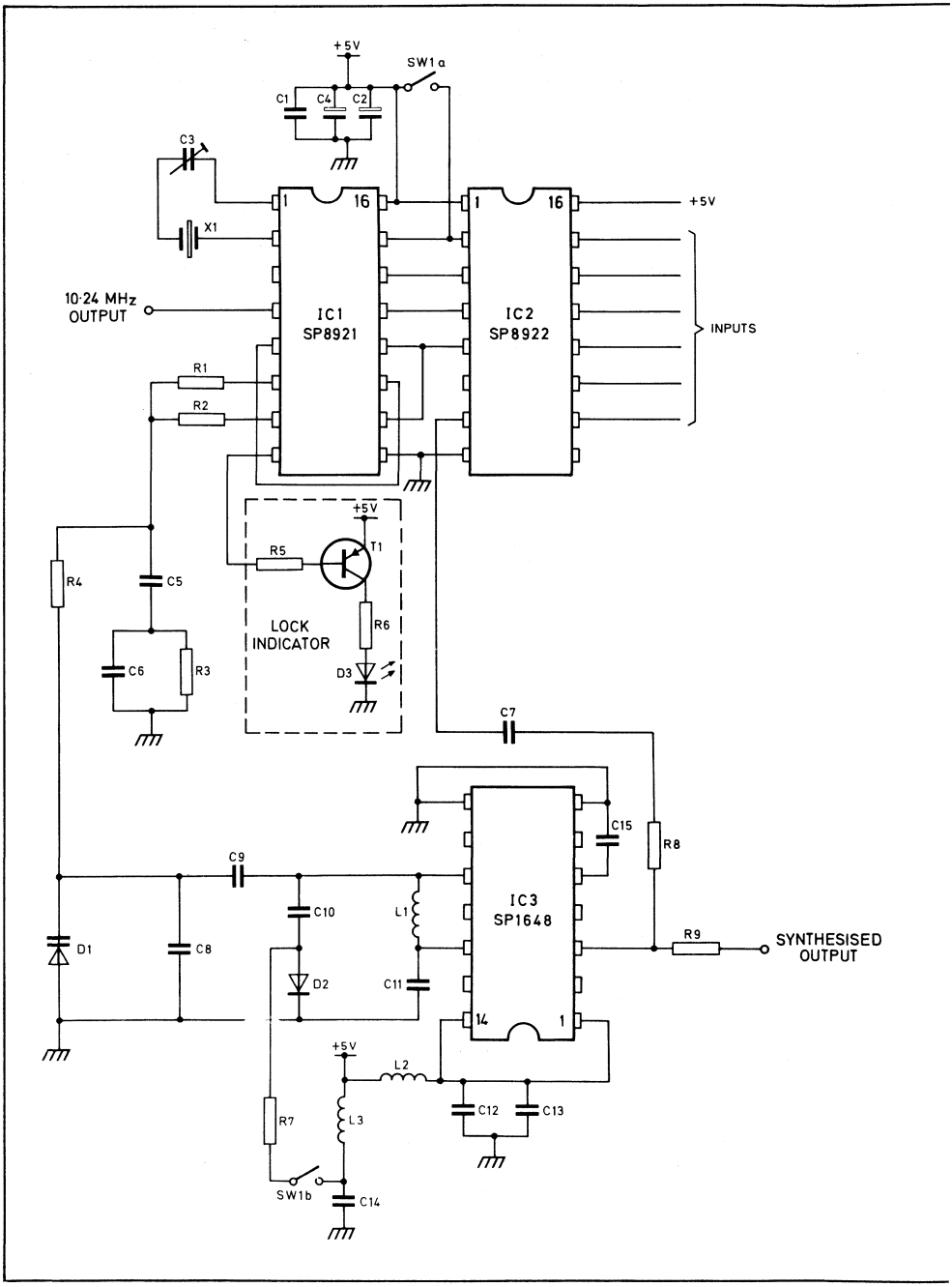
The programming inputs to the SP8922 are as shown in Table 4. Logic '1' is +3V or more, logic '0' is either ground or an open circuit. The circuit diagram of a programming input port is shown in Fig. 68. If a switch, constructed so as to select the correct combination for each channel, can be obtained this is the obvious way to program the synthesiser; otherwise a ROM may be suitably programmed and placed between the switch and the SP8922.

The crystal oscillator in the SP8921 is trimmed by a small variable capacitor, C3, which must be set up during alignment of the synthesiser so that the output frequency on pin 4 is 10.240000MHz. The only other adjustment is to set the core of L1 so that the varicap control voltage is 2.85V when the synthesiser is set to channel 30 transmit. Since the difference between transmit and receive frequencies is over 10MHz it is not possible to tune both with the same tuned circuit and an extra capacitor is switched by means of a diode during reception.

The phase/frequency comparator of the SP8921 can have an output swing from 0.5V to 3.8V but it is better to work in the range 1.5V to 3.0V as the phase-error output voltage is more linear in this region. The ZC822 tuning diode specified for this synthesiser may be replaced by any other tuning diode provided it will tune the VC0 over the required range, or a little more, as the control voltage goes from 1.5 to 3.0V. With slight coil changes the MV2105 has been used successfully in this synthesiser.

Channel No.	Input Code F E D C B A	Output frequency with R/T = 0 (MHz)
1	0 0 0 1 1 1	26.965
2	0 0 1 0 0 0	26.975
3	0 0 1 0 0 1	26.985
4	0 0 1 0 1 1	27.005
5	0 0 1 1 0 0	27.015
6	0 0 1 1 0 1	27.025
7	0 0 1 1 1 0	27.035
8	0 1 0 0 0 0	27.055
9	0 1 0 0 0 1	27.065
10	0 1 0 0 1 0	27.075
11	0 1 0 0 1 1	27.085
12	0 1 0 1 0 1	27.105
13	0 1 0 1 1 0	27.115
14	0 1 0 1 1 1	27.125
15	0 1 1 0 0 0	27.135
16	0 1 1 0 1 0	27.155
17	0 1 1 0 1 1	27.165
18	0 1 1 1 0 0	27.175
19	0 1 1 1 0 1	27.185
20	0 1 1 1 1 1	27.205
21	1 0 0 0 0 0	27.215
22	1 0 0 0 0 1	27.225
23	1 0 0 1 0 0	27.255
24	1 0 0 0 1 0	27.235
25	1 0 0 0 1 1	27.245
26	1 0 0 1 0 1	27.265
27	1 0 0 1 1 0	27.275
28	1 0 0 1 1 1	27.285
29	1 0 1 0 0 0	27.295
30	1 0 1 0 0 1	27.305
31	1 0 1 0 1 0	27.315
32	1 0 1 0 1 1	27.325
33	1 0 1 1 0 0	27.335
34	1 0 1 1 0 1	27.345
35	1 0 1 1 1 0	27.355
36	1 0 1 1 1 1	27.365
37	1 1 0 0 0 0	27.375
38	1 1 0 0 0 1	27.385
39	1 1 0 0 1 0	27.395
40	1 1 0 0 1 1	27.405

Table 4 SP8922/1 O/P frequencies with 10.240 crystal (0 = contact open, 1 = contact closed to V_{CC})


+5V
SW1a
C1
C4
C2
C3
X1
1
16
IC1
SP8921
IC2
SP8922
+5V
INPUTS
10·24 MHz
OUTPUT
R1
R2
R4
C5
C6
R3
+5V
R5
T1
LOCK
INDICATOR
R6
D3
C7
C15
R8
C9
C10
L1
IC3
SP1648
D1
C8
D2
C11
R9
SYNTHESISED
OUTPUT
14
1
+5V
L2
R7
L3
C12
C13
SW1b
C14

All resistors are in ohms and $\frac{1}{8}$W $\pm$ 10% unless otherwise stated. Capacitor values are in microfarads unless otherwise stated.

IC1	SP8921
IC2	SP8922/SP8923
IC3	SP1648
T1	2N 3906
D1	ZC822, Ferranti varactor diode
D2	1N4148 Silicon diode
D3	LED lock indicator
X1	10.240MHz crystal, series mode
L1	11 turns 30 gauge cotton covered wire on Neosid A7 assembly
L2	100 microhenries RF choke
L3	100 microhenries RF choke
R1	1.0k $\pm$ 5%
R2	1.0k $\pm$ 5%
R3	8.2k $\pm$ 5%
R4	33k
R5	10k
R6	150 (adjust for LED brightness)
R7	1k
R8	1k
R9	470 (adjust for required output level)
C1	0.1
C2	100, 10V solid tantalum
C3	2 – 22pF variable
C4	100 10V solid tantalum
C5	110V solid tantalum
C6	0.1
C7	1000pF
C8	22pF + 10%
C9	0.01
C10	100pF $\pm$ 10%
C11	0.01
C12	0.1
C13	10 solid tantalum
C14	0.1
C15	1000pF
SW1	2 pole, 1 way switch, (receive/transmit)

Offset	SP8921	SP8922
0	0	0
–455kHz	0	1
–10.240MHz	1	0
–10.695MHz	1	1

Table 5

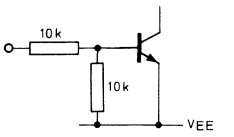


Fig. 68 Program input circuit

The low pass filter of the PLL consists of C5, C6 and R3. If faster lock (at the expense of larger noise and reference sidebands) is required the filter may be redesigned. If the synthesiser is used in a scanning receiver, a switched filter should be used to give fast lock during scanning but a slower lock and cleaner signal during normal operation. The lock output on pin 8 of the SP8921 is used to light an indicator when the loop is *not* locked and should also be used, in a transmitter or transceiver, to prevent transmission when the loop is unlocked.

Fig. 69 shows the circuit board layout and component placing of this synthesiser. It requires a single +5V supply and draws about 60mA. The performance is improved if double-sided board is used with a ground plane on one side. A small further improvement would come from the use of a grounded screening can over the whole system.

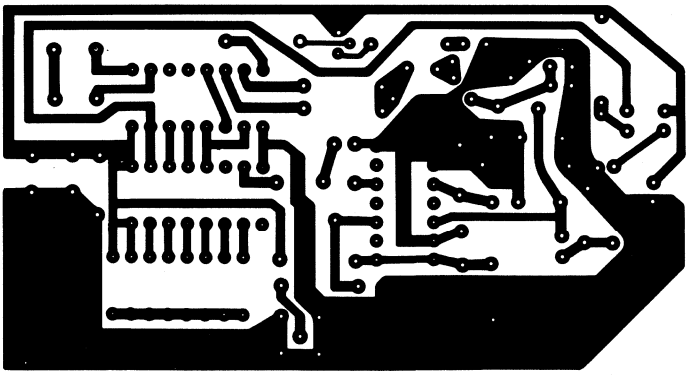


Fig. 69a Printed circuit layout for CB synthesiser

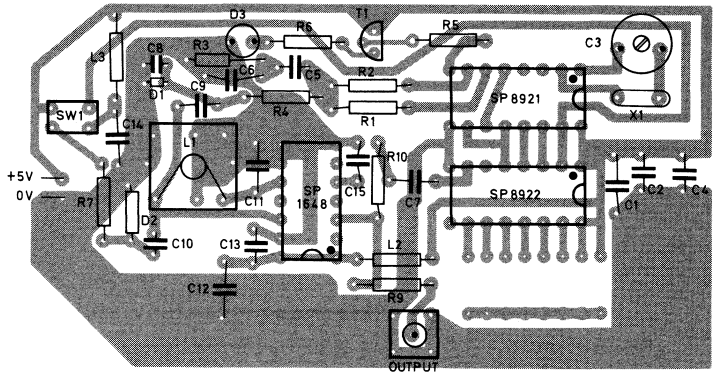


Fig. 69b PCB component layout for CB synthesiser

The synthesiser has reference frequency sidebands 50dB down at 1.25kHz from the carrier. All output over 5kHz from the carrier is over 70dB down. Lock time for a change from channel 0 to channel 40 (a frequency change of 440kHz) is around 35ms. Photographs of the output spectrum and the change of control voltage with time during a step from channel 0 to channel 40 are shown in Fig. 70.. Stepping from transmit to receive or vice versa takes somewhat longer because of the much larger change of frequency but is generally complete within 75ms.

This synthesiser is quite basic but has adequate performance for the majority of CB applications. If improved performance is required there are two possibilities; an improved FET oscillator having lower floor noise instead of the SP1648 or an improved low pass filter to reduce reference frequency sidebands.

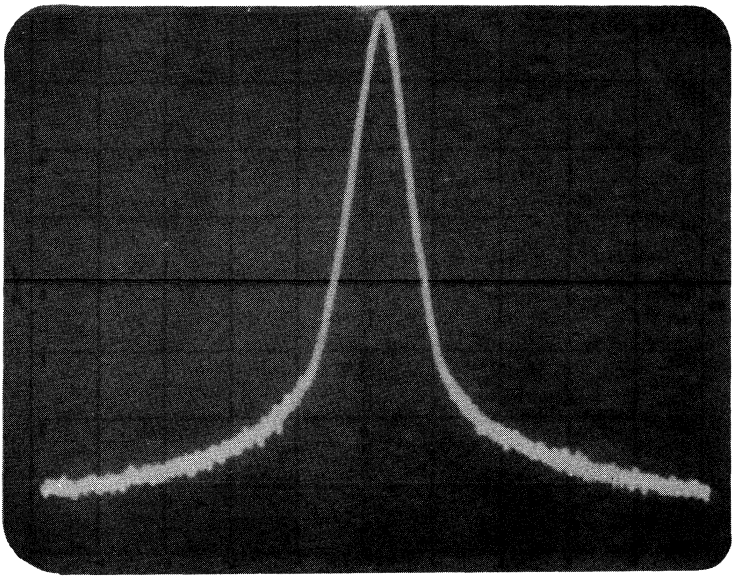


Fig. 70a Typical output spectrum of basic synthesiser (Vert.:16dB/div.,Horiz.:2kHz/div.,) BW:300Hz, fo:27.065MHz

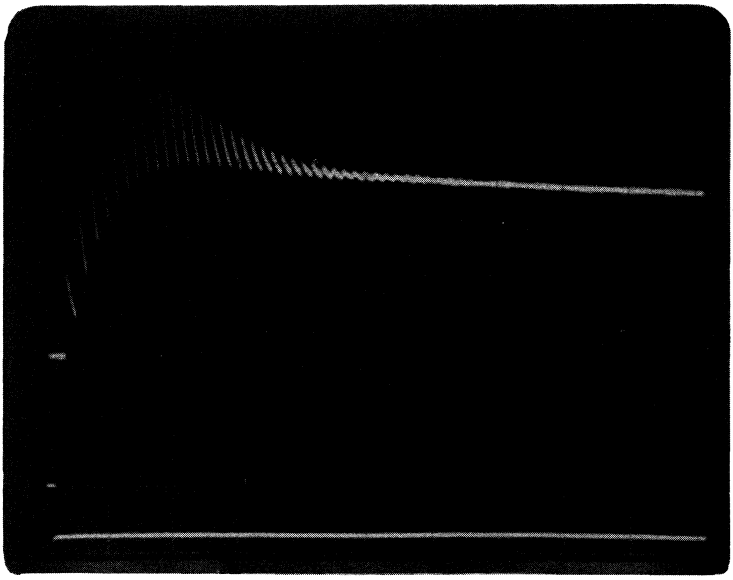


Fig. 70b Typical transient response of basic synthesiser. Response of varactor line to step program change 1–40. Vert.:200mV/div.,Horiz.:5ms/div. N.B. Droop of response is due to the measuring instrument being AC-coupled.

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